环形正负电子对撞机
Circular Electron Positron Collider

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A compact CMOS pixel design for the CEPC vertex detector

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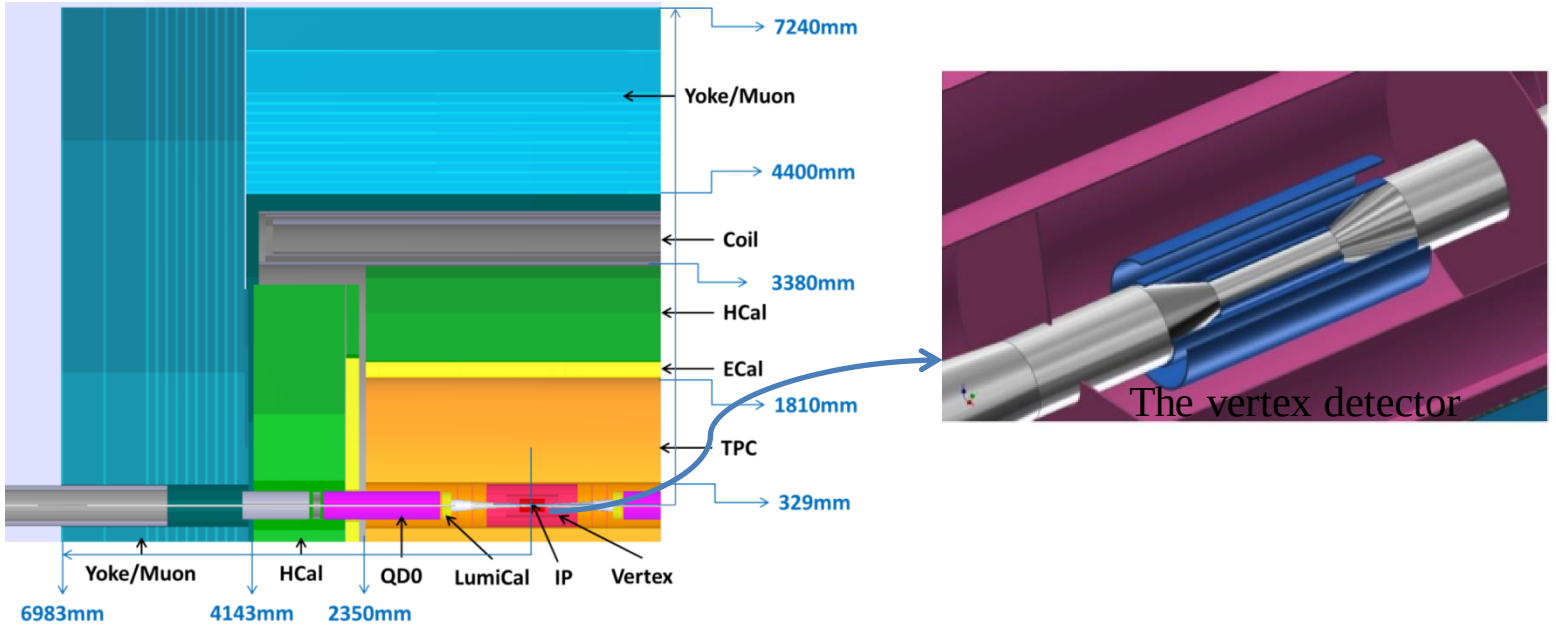
On behalf of the CEPC VTX study group

The 2019 international workshop on the high energy CEPC
Nov, 18-20 2019

Outline

- CEPC vertex detector and design specifications
- CPS development and the prototypes
  - Sensitive diode study
  - First prototype of an asynchronous readout mode and test results
  - A more compact prototype design of rolling-shutter readout mode
- Summary

Detector Layout



Vertex detector:

- Single point resolution near the IP: $\leq 3\ \mu m \rightarrow$ *high granularity*
- material budget: $\leq 0.15\% X_0/layer \rightarrow$ *Low power dissipation, thinned, monolithic pixel sensor*
- pixel occupancy: $\leq 1\% \rightarrow$ *High granularity and/or short readout time*
- Radiation tolerance: $\sim$1Mrad/y (TID) and $\sim 10^{12}$ $N_{eq}/cm^2/y$ (NIEL)

Design specification

◆ **Generally require：**

- **High granularity, σ = 3-5 μm;**
- **thin pixel sensors with fast readout, readout time = 10 -100 μs ;**
- **and low power dissipation, Power < 100 mW/cm^2**

◆ **Spatial resolution**

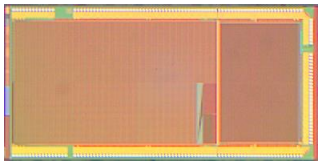
- $\frac{0.5\text{pitch}}{\sqrt{12}}$ **< S.P.resolution <** $\frac{\text{pitch}}{\sqrt{12}}$
- **若 S.P.resolution = 3 μm，10.3 μm < pitch < 20.7 μm**

◆ **Low power**

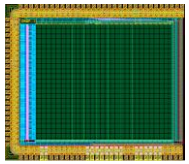
- **Binary circuit inside pixel**
- **Inside matrix zero-suppression readout, but have large pixel pitch**

Developed CMOS Pixel Sensor prototypes for CEPC

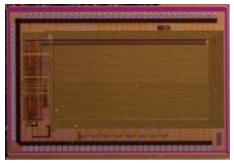
Prototype	Pixel size (μm^2)	Collection diode bias (V)	In-pixel circuit	R/O architecture	Main goals	Status
JadePix1	33 × 33 16 × 16	< 1.8	SF/amplifer, analog output	Rolling shutter	Sensor optimization	Lab. and beam test finished
JadePix2	22 × 22	< 10 V (ac-coupled)	amp., discriminator, binary output	Rolling shutter	Small pixel, Power < 100 mW/cm^2	Electrical functionality verified
MIC4	25 × 25	reverse bias	Low power front-end, address encoder	Data-driven, Asynchronous	Small pixel, fast readout	Electrical functionality verified
TaiChuPix1	25 × 25	reverse bias	Low power front-end, address encoder	Data-driven, Asynchronous	Small pixel, fast readout with time stamp	In measurement
JadePix3	16 × 26 16 × 23.11	reverse bias	Low power front-end, binary output	Rolling shutter with end of col. priority encoder	Small pixel, low power	In fabrication



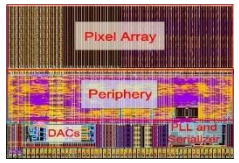
JadePix1 (IHEP)
3.9 × 7.9 mm^2



JadePix2 (IHEP)
3 × 3.3 mm^2



MIC4 (CCNU & IHEP)
3.2 × 3.7 mm^2

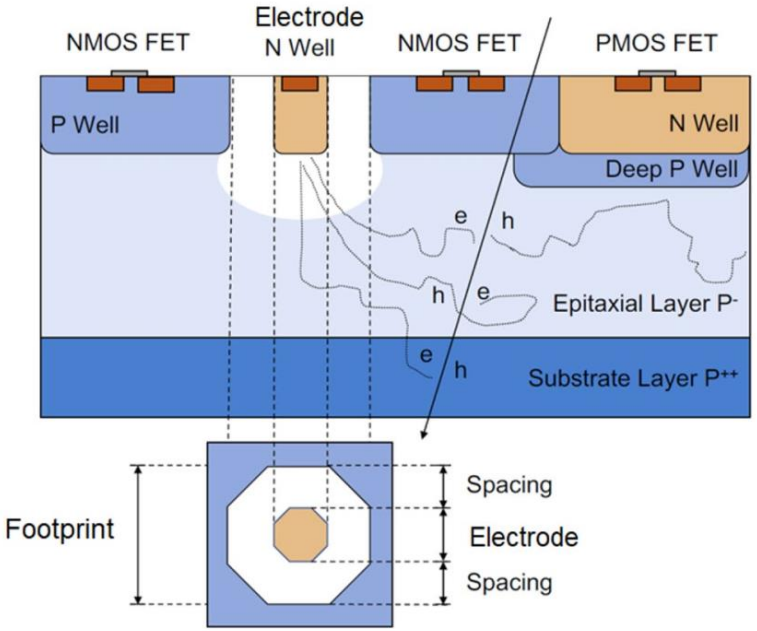


TaiChuPix1 (IHEP, SDU, NWPU, IFAE, CCNU)
5× 5 mm^2

JadePix3(IHEP, CCNU, Dalian Minzu Unv., SDU)
10.4 × 6.1 mm^2

All prototypes in TowerJazz 180 nm CIS process

Lower input C lower analog power



$$N \propto \frac{1}{\sqrt{g_m}} \qquad S = \frac{Q}{C}$$

$$\frac{S}{N} \propto \frac{Q}{C}\sqrt{g_m} \propto \frac{Q}{C}\sqrt[2a]{I}$$

$$g_m \propto I^{\frac{1}{a}}$$

a = 2 in strong inversion
a = 1 in weak inversion

Assuming that main analog power dissipation comes from the input transistor bias

$$P \propto I \propto \left(\frac{S/N}{Q/C}\right)^{2a}$$

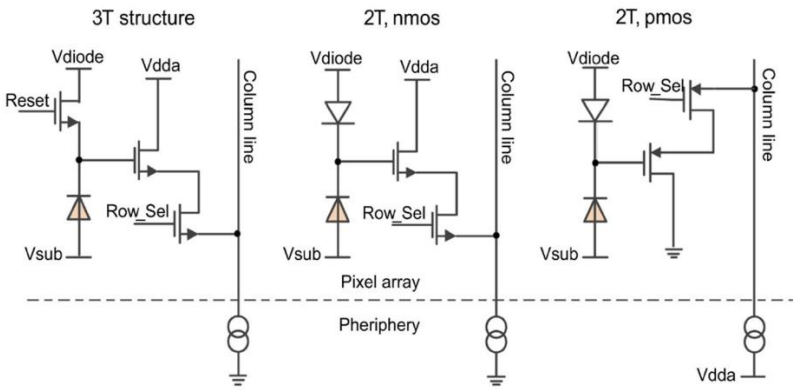
C ↓

Fixing the S/N for a given bandwidth
higher Q/C allows for a lower power

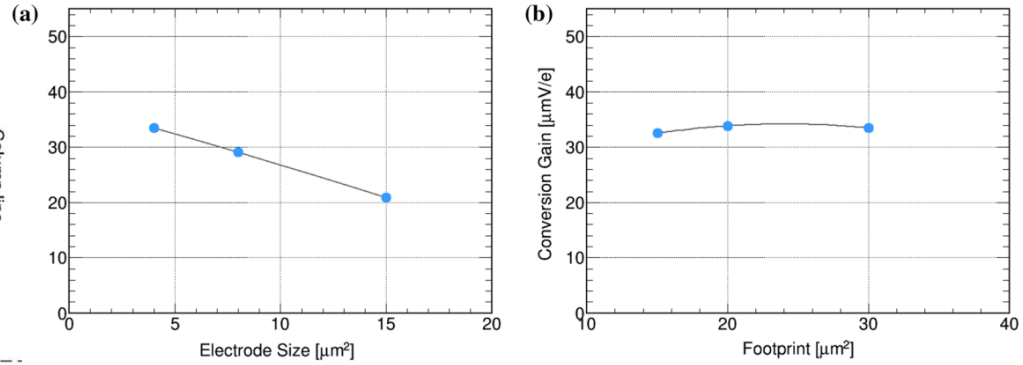
Y.Zhang, et al, NIMA 831(2016) 99-104

Sensitive diode test results

- Goals: sensitive diode geometry optimization with JadePix1

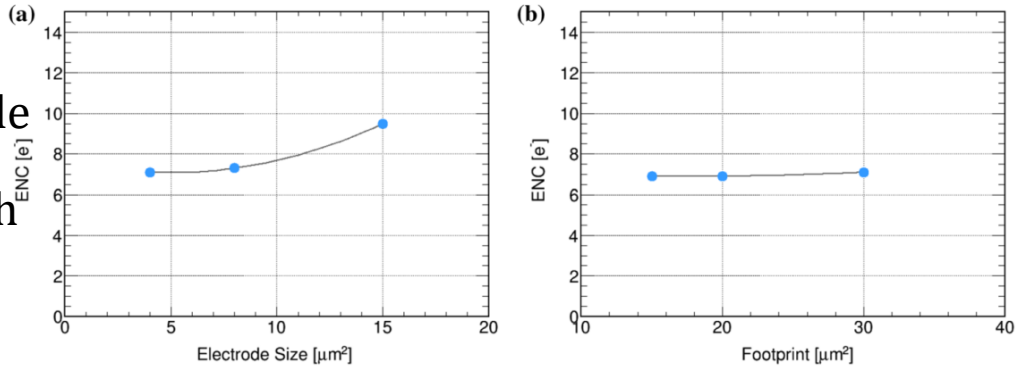


(a)sensitive diode test circuit scheme



(b) conversion gain VS. sensor geometry

- Conclusion: Small collection electrode size and large footprint can achieve high charge-over-capacitance ratio.

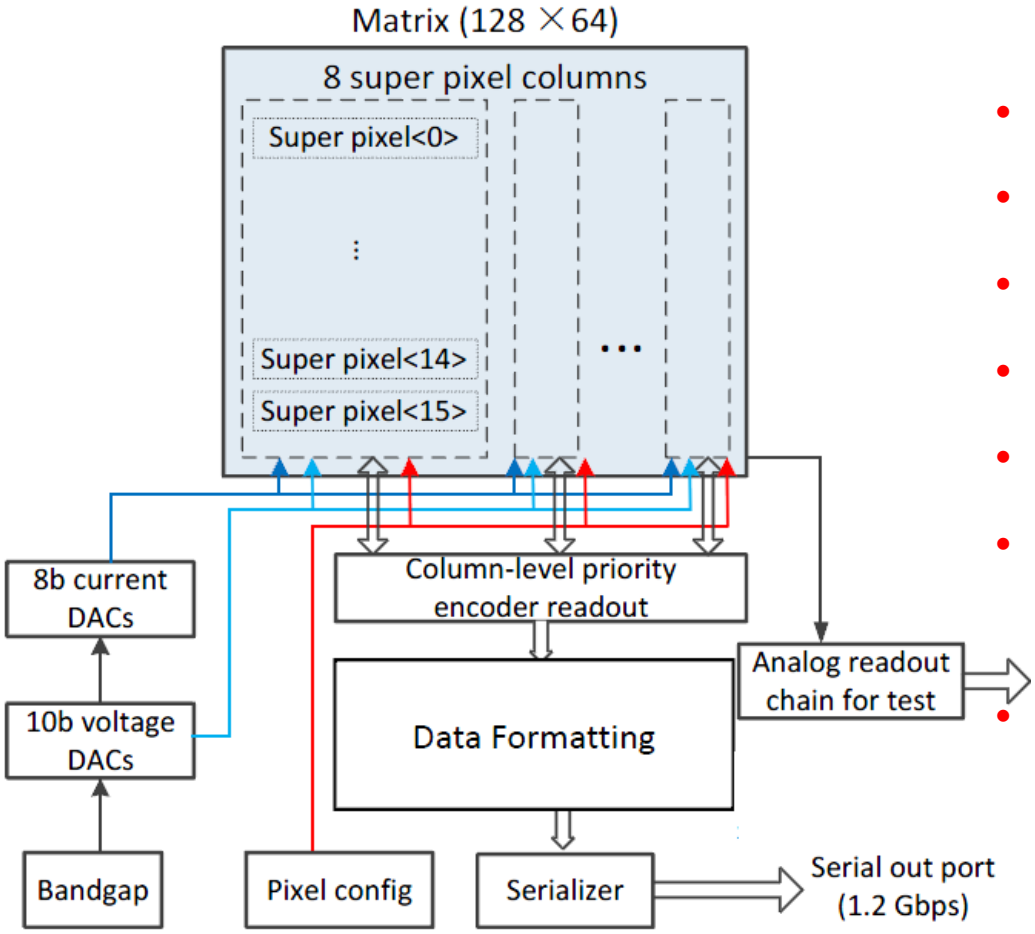


(C) ENC VS. sensor geometry

L.J.Chen, et al, RDTM (2019)
DOI: 10.1007/s41605-019-0124-0

First prototype MIC4 overall introduction

- Goals: ① To explore a new data-driven readout architecture which can be implemented into a small pixel size; ② Front-end study. ③ Periphery block.

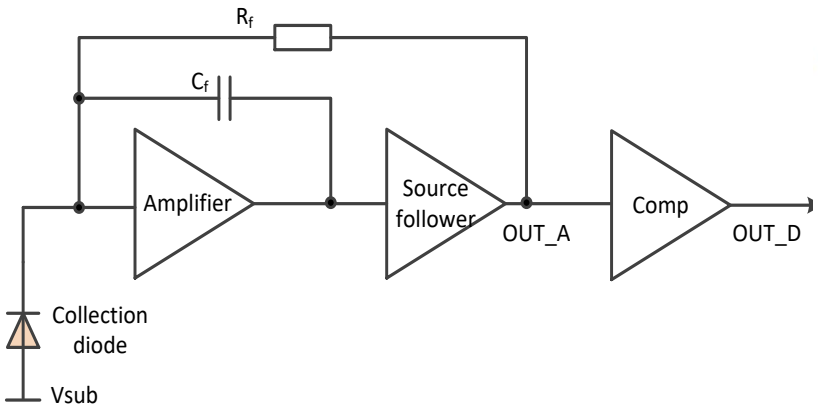


(a) MIC4 structure (MAPS IN CCNU4)

- Pixel size: 25 um x 25 um
- Matrix: 128 rows x 64 columns
- Two different front-ends in the matrix
- Zero suppression readout inside matrix
- DACs, bias
- No memory in the periphery, real time readout, serial readout rate 1.2 Gbps
- Analog test for the last row pixels

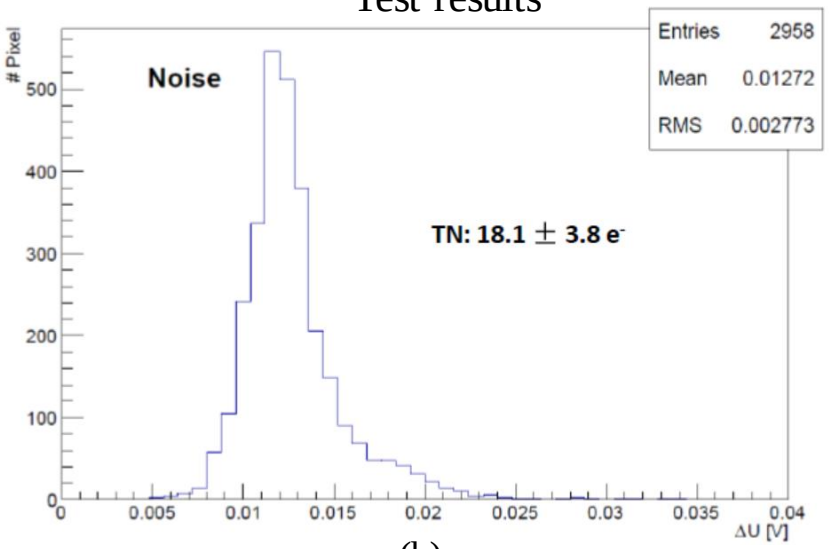
P. Yang, et al., NIM-A 924 (2019) 82-86

MIC4:Pixel digital front-end version 1

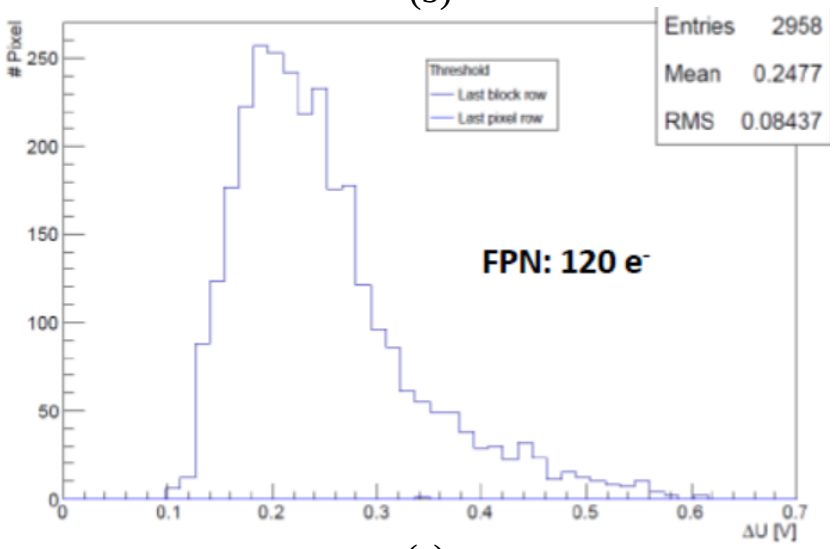


(a) CSA based analog front-end V1
by Ying ZHANG @ IHEP

Test results



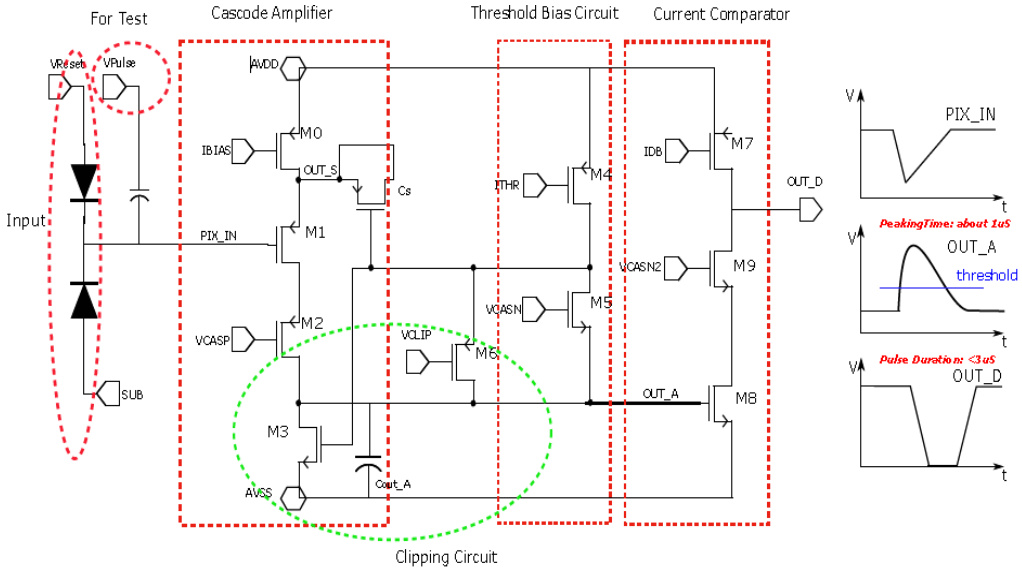
(b)



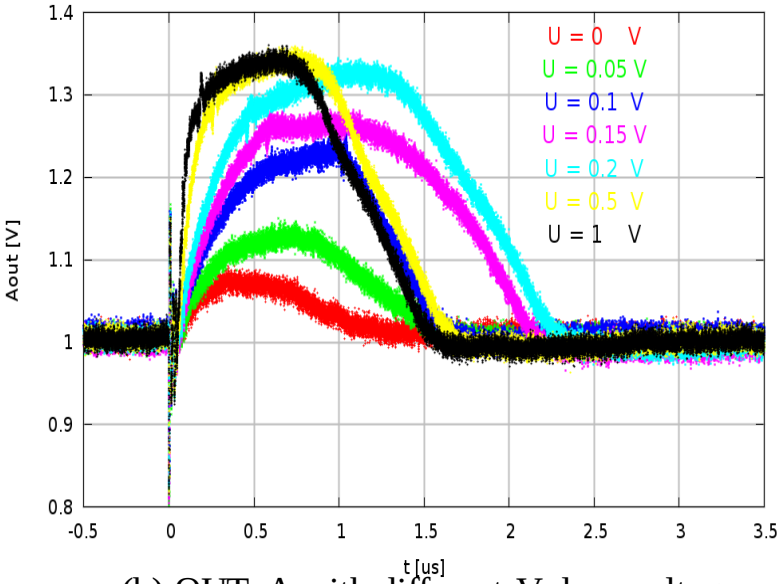
(c)

- Power cons.: 35 nW/pixel
- TN noise 18 e- is consistent with the sim results, but FPN noise 120e- is much larger than simulation (mismatch).

MIC4:Pixel digital front-end version 2

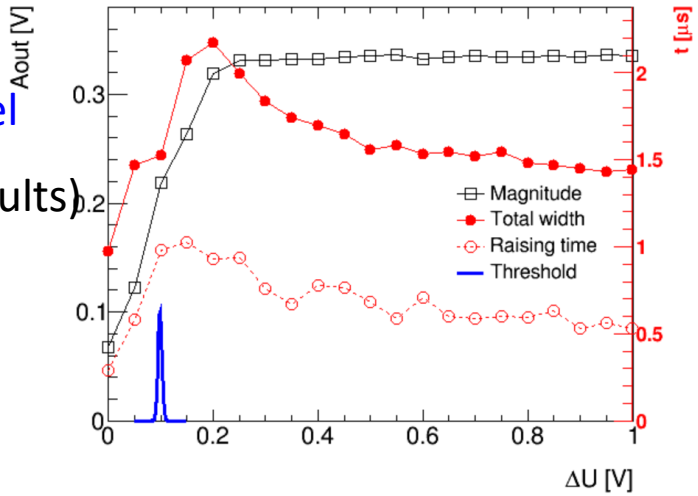


(a)Front-end V2 based on ALPIDE by Weiping Ren @ CCNU



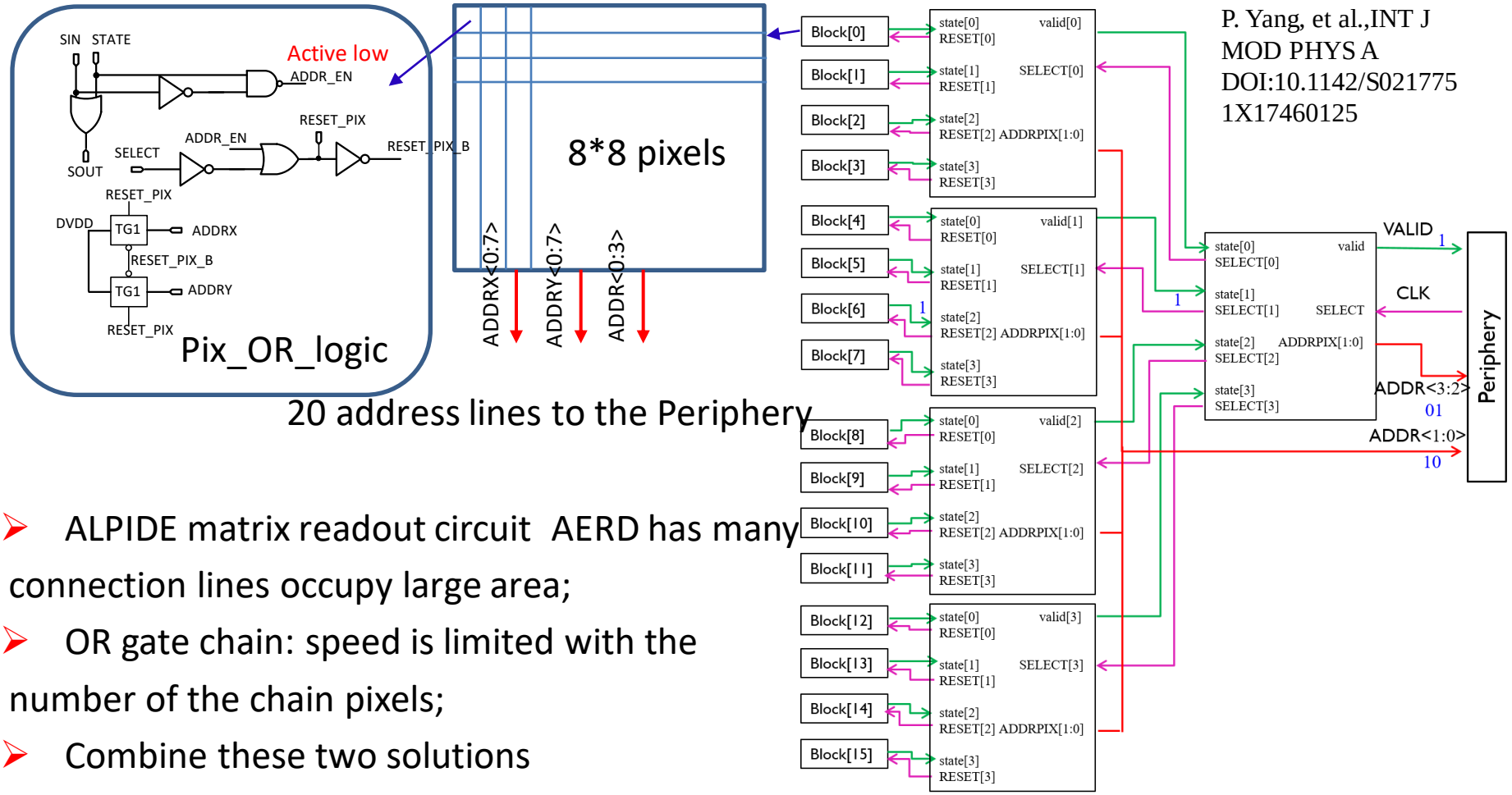
(b) OUT_A with different Vpluse voltage

- The ALPIDE front-end structure, Power: 110 nW/pixel
- Peaking time< 1 μs, duration < 3 μs (sim and test results)
- Mean threshold around 99 e- (test results)
- Mean FPN ~ 31 e-, TN ~ 6 e- (test results)



(c) Test results of peaking time and duration time

MIC4 data-driven readout scheme



P. Yang, et al.,INT J MOD PHYS A
DOI:10.1142/S021775
1X17460125

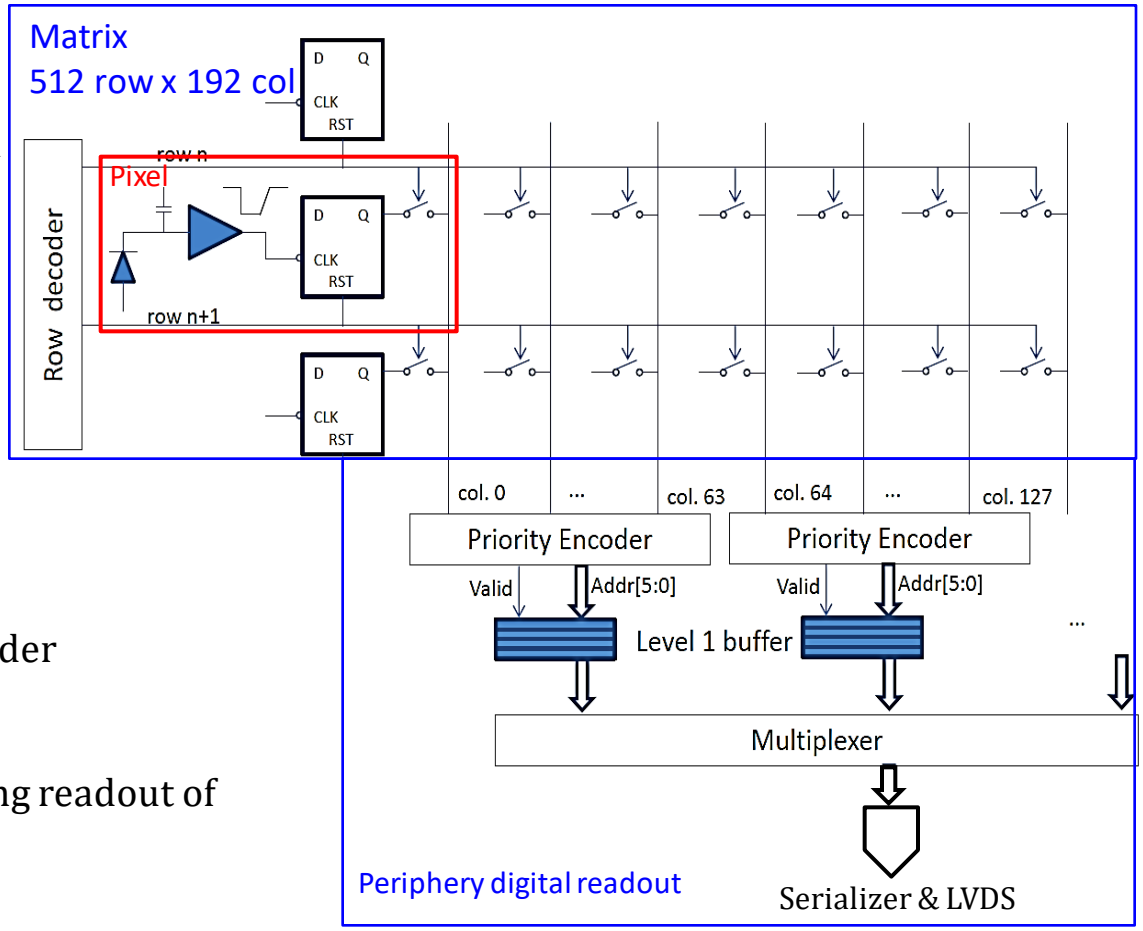
20 address lines to the Periphery

- ALPIDE matrix readout circuit AERD has many connection lines occupy large area;
- OR gate chain: speed is limited with the number of the chain pixels;
- Combine these two solutions
- Digital periphery provide a CLK signal of 60% duty cycle to enhance the readout circuit to work at 40 MHz to decode 1024 pixels; -> a few μs readout time

JadePix3: Prototype of small pixel design

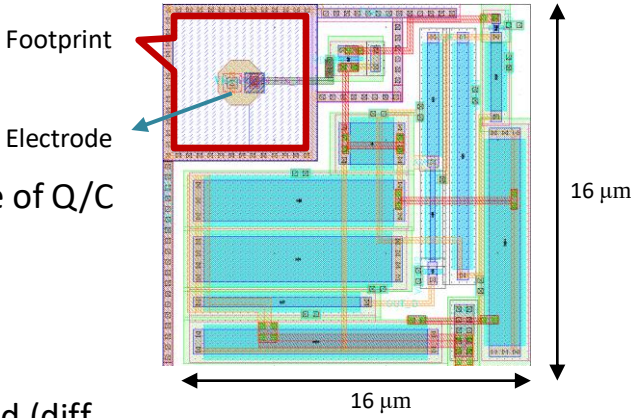
- Goal: Small pixel size → Low power FE + Rolling shutter Readout

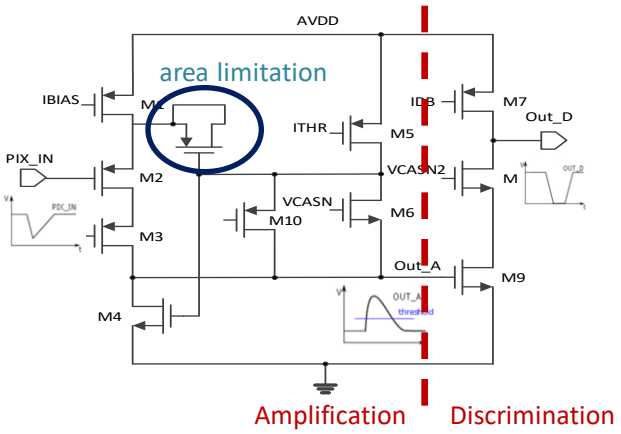
- In-pixel circuit
  - Low power binary front-end
  - Optimized DFF
- Matrix Readout
  - Rolling shutter
  - 200ns/row
- Periphery digital Readout:
  - Shared column lines
  - End of column Priority Encoder
    Zero suppression
  - 64 columns processed during readout of one row

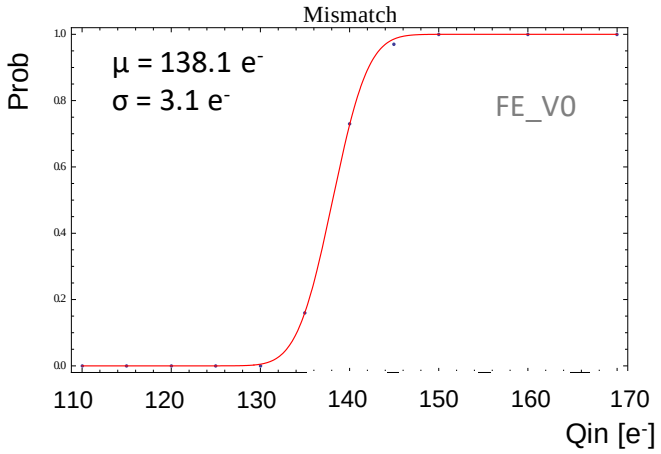


JadePix3:Sensor & Front-end design

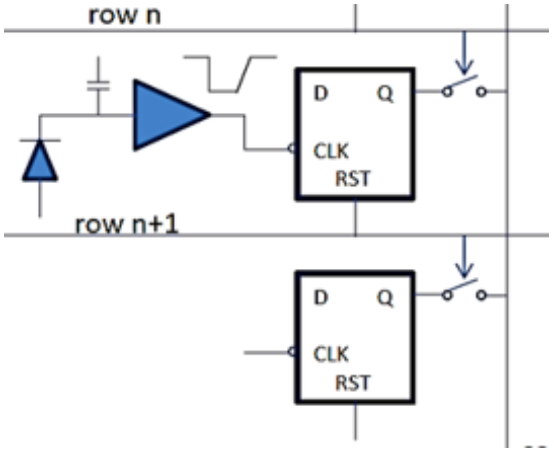
- Design goals: small pixel size and low power consumption
- Sensor: High Q/C (collected charge/sensor capacitance) ➔ **low power**
  - Electrode size of 4 μm^2, with a large footprint of 36 μm^2 → compromise of Q/C with area
- Front-end:
  - Operating principle derived from ALPIDE front end, two version designed (diff. power & peaking time)
  - Reduction on layout area, ~210 μm^2
  - Improvement on the threshold dispersion (compromise with area)

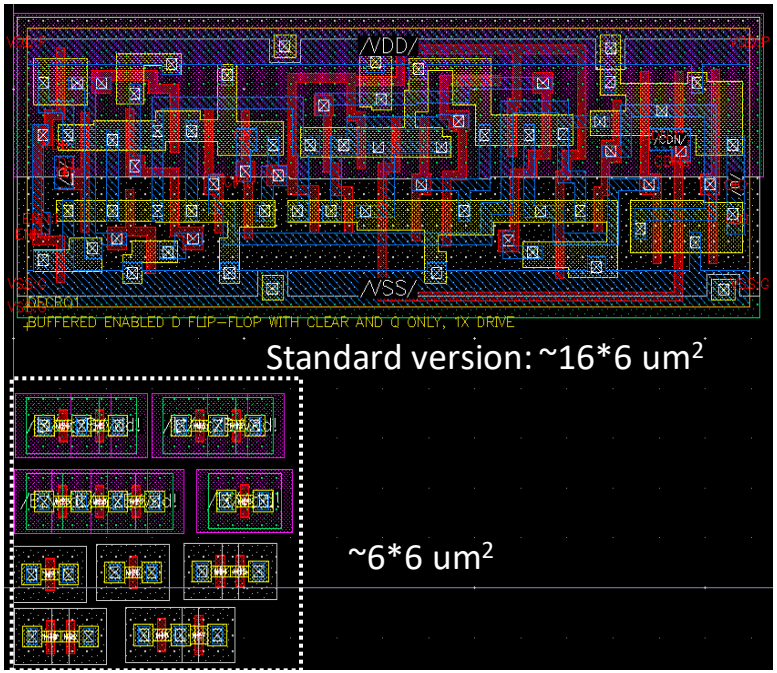






JadePix3: DFF optimized for compact pixel





Layout of modified DFF compared with standard version

In-pixel DFF Modified :

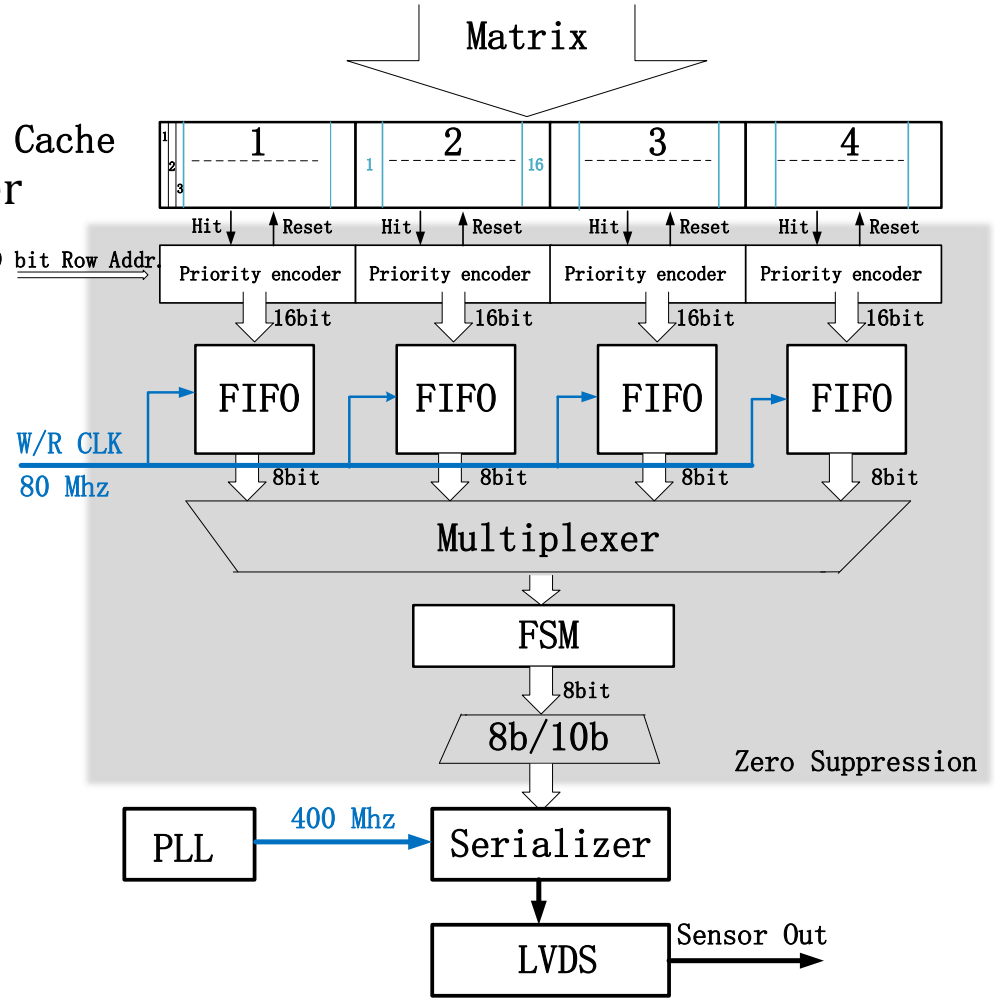
- Compared with standard version:
  - Transistor Num.: reduced from 36 → 16
  - Layout size: 16*6 μm² → 6*6 μm²
    (reduced >60%)
- D connect to ground;
- Signal input from pin CLK;
- One control line shared for:
  - RST of **row n** / Read of **row n+1**

JadePix3: Digital periphery readout

Zero suppression at the EOC

- Priority encoder and reset decoder
  - 4 bit address encoder * 4 Sectors
  - 3 Columns as one block
- Hit information 16bit:

  - 9 bit row Addr. + 4bit col. Addr. + 3bit hit (one-hot code)
- FIFO R/W clk: 80 MHz
- FIFO depth: 48
- Data after 8b/10b : 400Mhz
- Layout: ~ 5120 μm * 200 μm
- Power: 15.35 mW

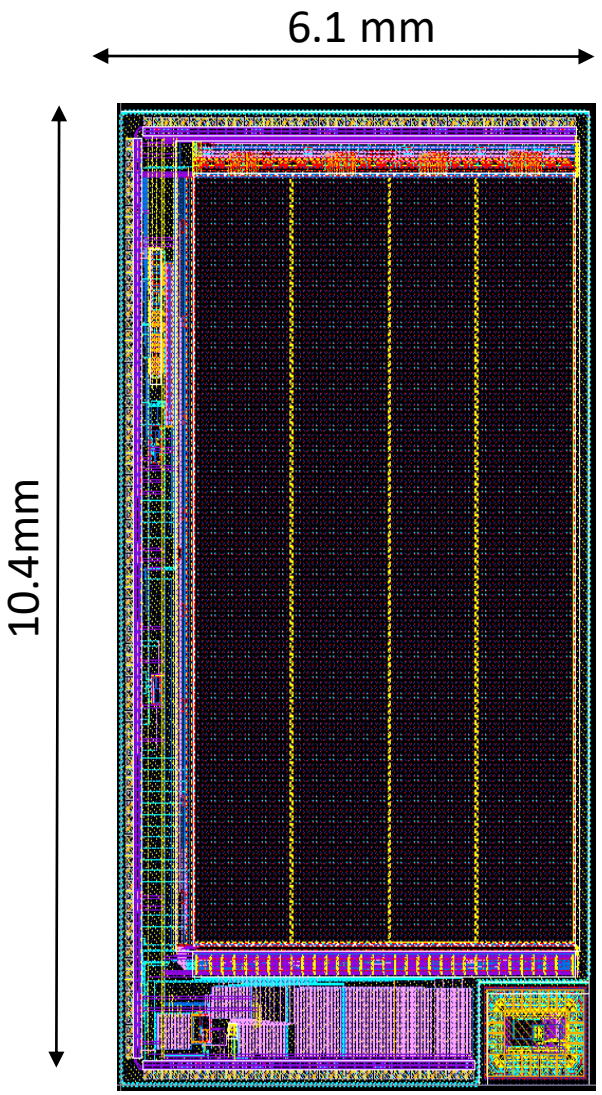


JadePix3: Status

Team IHEP, CCNU, Dalian Minzu Unv., SDU

- Submission in Sept. 2019
- Sensitive diode, minimum size
- Front-end based on ALPIDE, but 2 versions
  - FE_V0, FE_V1 (9mW/cm^2 , 26mW/cm^2)
- Pixel digital, 3 versions
  - DGT_V0，DGT_V1， DGT_V2
- Pixel area
  - 16×26 μm^2
  - 16×23.11 μm^2

Sector	Diode	Front-end	Pixel digital	Pixel layout
0	2 + 2 μm	FE_V0	DGT_V0	16×**26** μm^2
1	2 + 2 μm	FE_V0	DGT_V1	16× **26** μm^2
2	2 + 2 μm	FE_V0	DGT_V2	16× **23.11** μm^2
3	2 + 2 μm	FE_V1	DGT_V0	16×26 μm^2



Summary

- Sensitive diode geometry was studied, minimum sensitive area (JadePix1/2)
- Explored a new zero-suppression structure inside matrix, with low power front-end and almost full chip periphery blocks. All of the modules are functional. The threshold and noise was studied. (MIC4 chip)
- JadePix3 optimized the pixel size and chip periphery power consumption
  - Small pixel size, better spatial resolution expect ~3 um
- Radiation test and beam test is ongoing

Thanks to my colleagues:

IHEP: Yunpeng Lu, Ying Zhang, Yang Zhou, Zhigang Wu, Qun OuYang
CCNU: Xiangming Sun, Di Guo, Chaosong Gao,Le Xiao, Chenxing Meng, Anyang Xu
Dalian Minzu Unv: Zhan Shi
SDU: Liang Zhang

Thank you for your attention!