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# Present and future perspectives of depleted monolithic CMOS pixel sensors

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2019 International Workshop on the High Energy Circular Electron-Positron Collide

# Perspective

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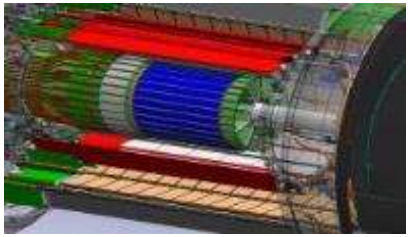
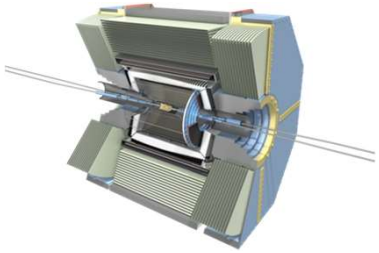
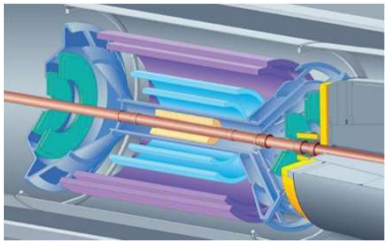
**STAR**



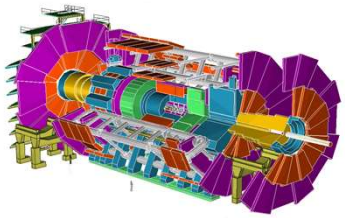
**Belle II**



**ALICE-(HL)-LHC**



**ATLAS**



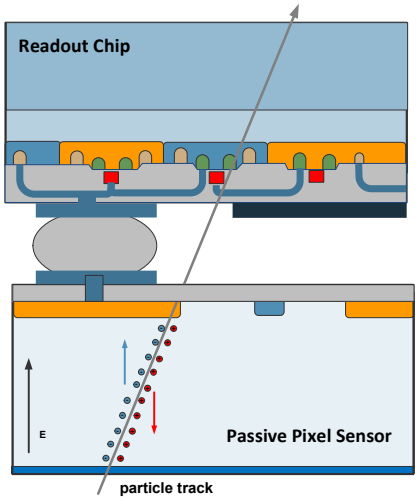
| | ALICE | ILC | LHC pp | HL-LHC-pp | | CEPC | Belle Upgrade |
|---|---|---|---|---|---|---|---|
| | | | | Outer | Inner | | |
| BX-time (ns) | 20 000 | 350 | 25 | **25** | **25** | **25**-760 | ~100 |
| Hit Rate (MHz/cm$^2$) | 1 | 25 | 100 | 100 | **4 000** | ~30 | 100-500 |
| $\Phi$ ($n_{eq}$/cm$^2$) * | > $10^{13}$ | $10^{12}$ | 2x$10^{15}$ | $10^{15}$ | **1x$10^{16}$** | < $10^{14}$ | < $10^{13}$ |
| TID (Mrad)* | 0.7 | 0.4 | 80 | 50 | **> 500** | 30-40 | 10-50 |
| Pitch (um$^2$) | 28x28 | | 50x250 | 50x50 | 50x50 | **16x16** | ~40x40 |

* for 10 years

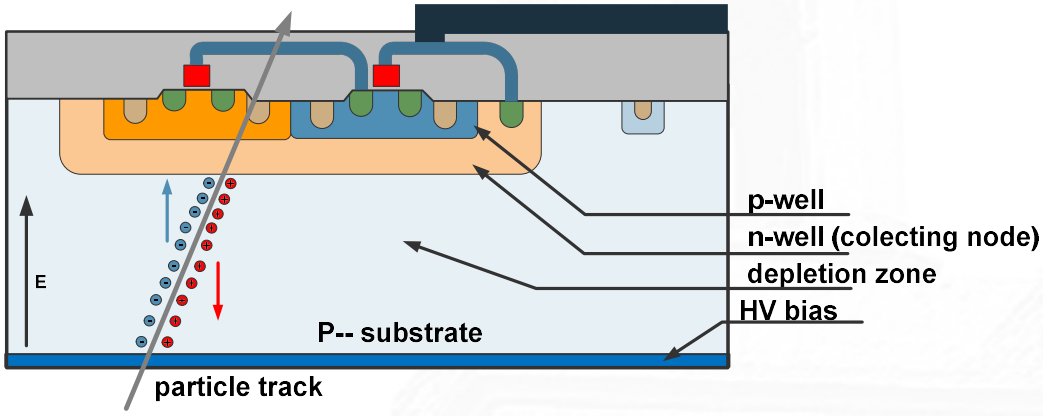
# Design for Sensor Radiation Tolerance

In the context of HL-LHC

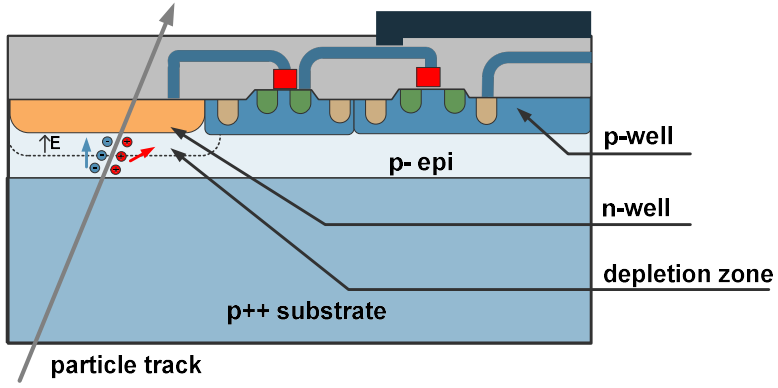
# Hybrid Pixel Detectors




# Depleted Monolithic Pixels

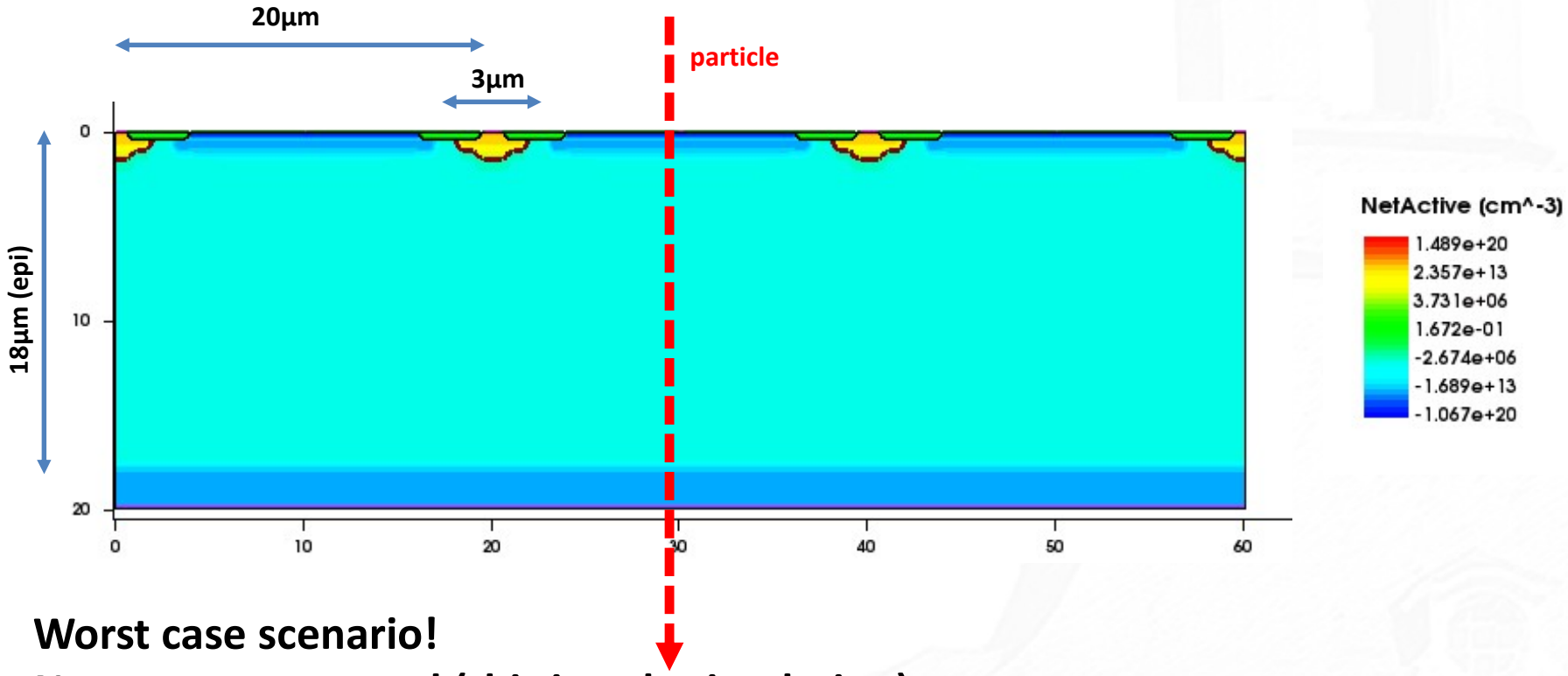



# Monolithic Pixels



# Sensor Design Paramters

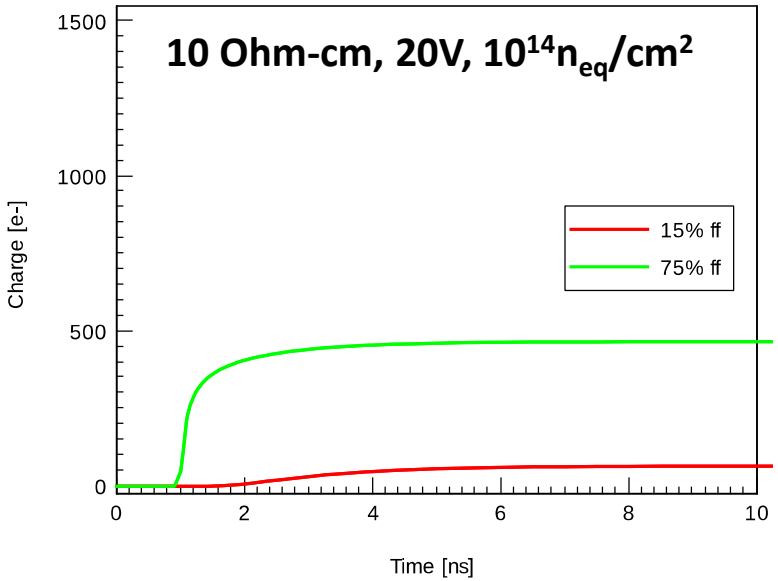
- Substrate doping concentration (resistivity)
- Maximum sensor bias voltage
- Geometry (thickness, fill-factor)

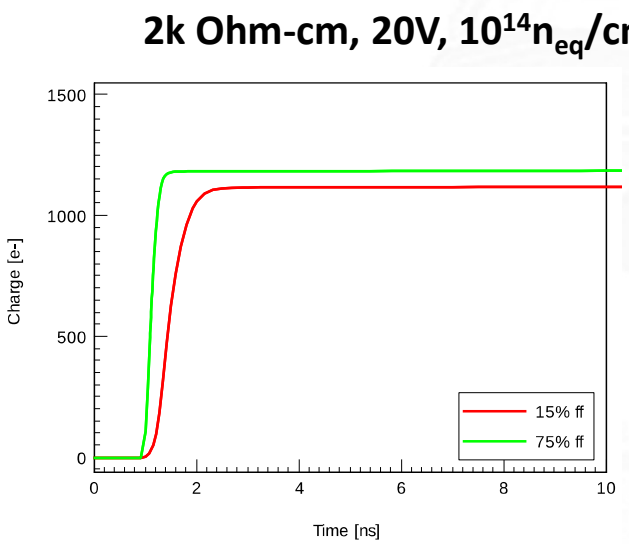


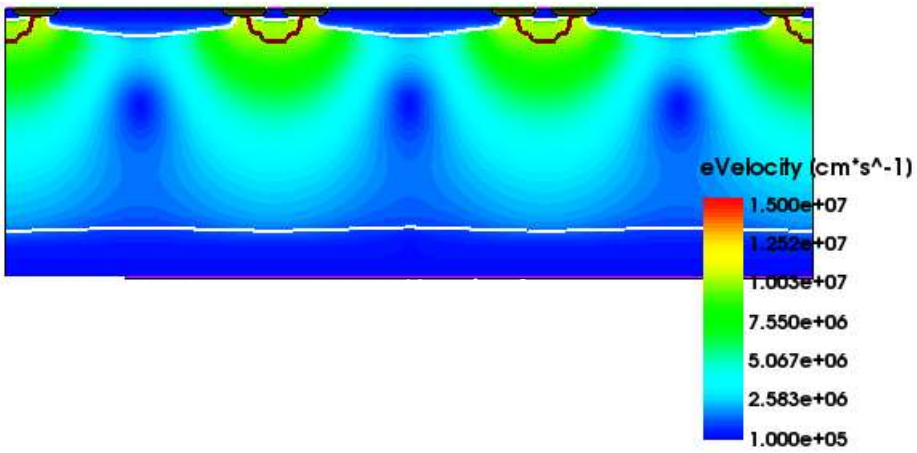

- **Worst case scenario!**
- **No acceptor removal (this is only simulation)**

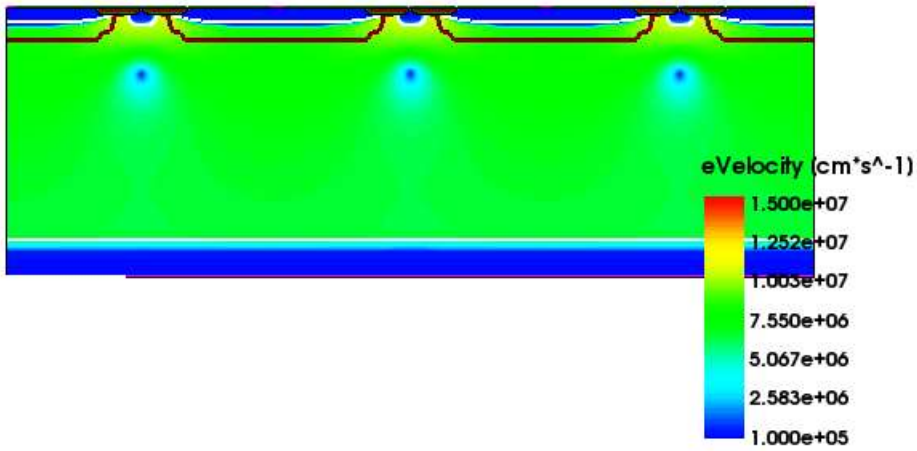
*Code: https://gitlab.cern.ch/TCADExamples/ChargeCollection*

# Geometry/Fill Factor

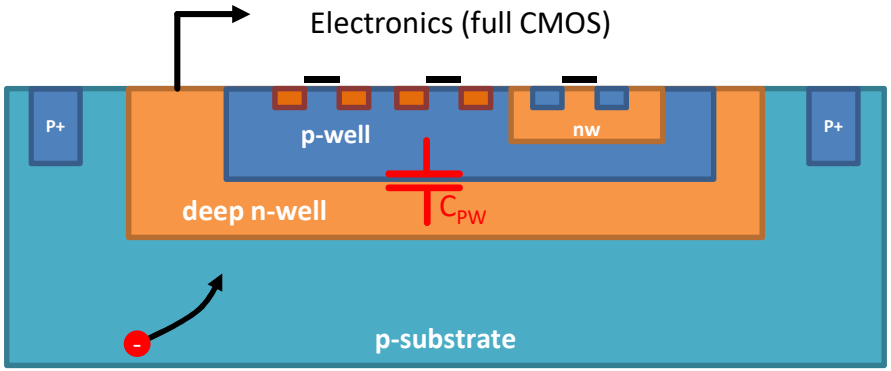


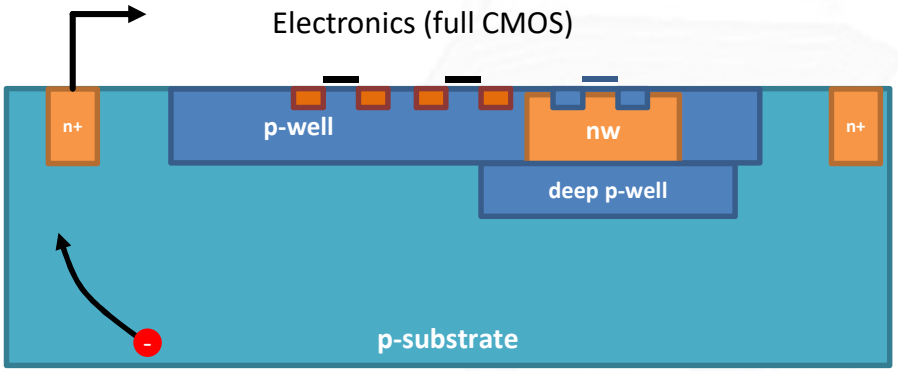



# Fundamental process options




Electronics **inside** charge collection well

- Collection node with **large fill factor** → rad. hard
- Large sensor capacitance (DNW/PW junction!) → x-talk, noise & speed (power) penalties
- Full CMOS with isolation between NW and DNW

Electronics **outside** charge collection well

- Very **small sensor capacitance** → low power
- Potentially less rad. hard (longer drift lengths)
- Full CMOS with additional deep-p implant
- **Smaller pitch**

**input capacitance** vs **electric filed**

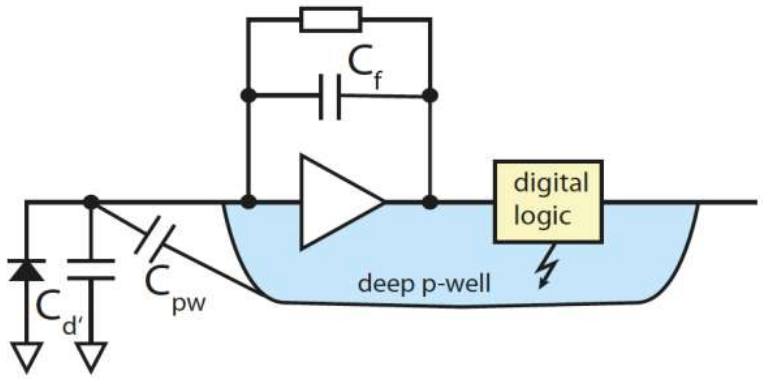
**power** vs **radiation**

*I. Peric, DOI: 10.1016/j.nima.2007.07.115*
*T. Kishishita, et al., DOI: 10.1088/1748-0221/10/03/C03047*
*P. Rymaszewski, et al., DOI: 10.1088/1748-0221/11/02/C02045*
*T. Hirono, et al., DOI: 10.1109/NSSMIC.2016.8069902*

*R. Turchetta, et al., DOI: 10.1016/S0168-9002(00)00893-7*
*W. Dulinski, et al., DOI: 10.1109/TNS.2004.832947*
*A. Dorokhov , et al., DOI: 10.1016/j.nima.2010.12.112*
*M. Havránek, et al., DOI: 10.1088/1748-0221/10/02/P02013*

# Consequences of the additional inter-well capacitance

- larger total detector capacitance: $\mathbf{C_d} = C_{d'} + C_{pw}$




- noise $ENC^2_{thermal} \propto \frac{4}{3}\frac{kT}{g_m}\frac{\mathbf{C_d^2}}{\tau}$
- timing $\tau_{CSA} \propto \frac{1}{g_m}\frac{\mathbf{C_d}}{C_f}$

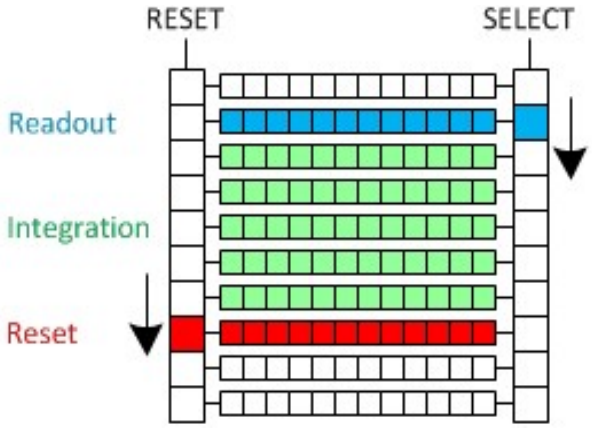
need to increase $g_m$ to compensate
=> increased power ($g_m \propto I_d$)

- cross talking into sensor
  The PW/DNW capacitance $C_{pw}$ directly couples into the sensor (the CSA input node).
  Even with careful layout and low noise digital circuitry the operation threshold can be affected.
  For example: for $C_{pw}$ = 100 fF, $\Delta V_{pw}$ = 1mV => $Q_{x\text{-}talk}$ = 625 $e^-$

# Readout

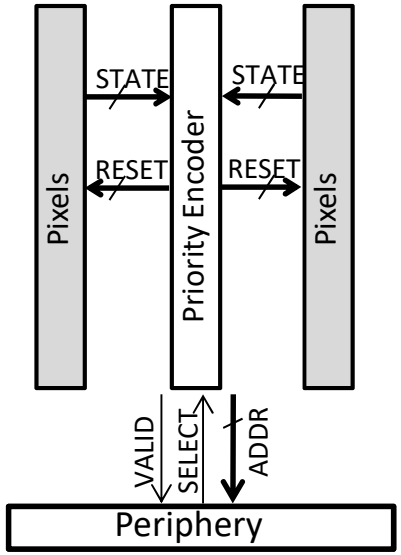
# Readout concepts

## Rolling Shutter



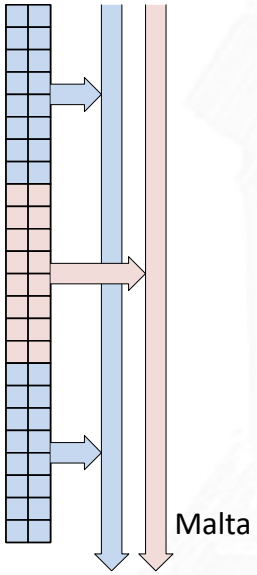

MIMOSA
PXD/DEPFET

## Priority Encoder



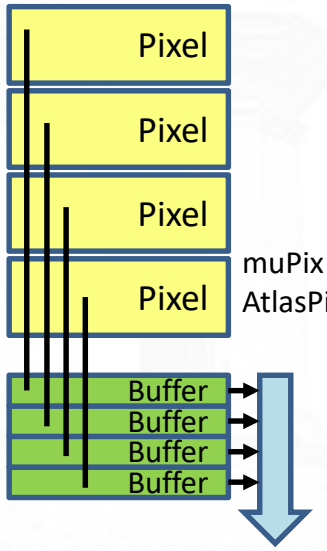

Alpide

## Shared Bus



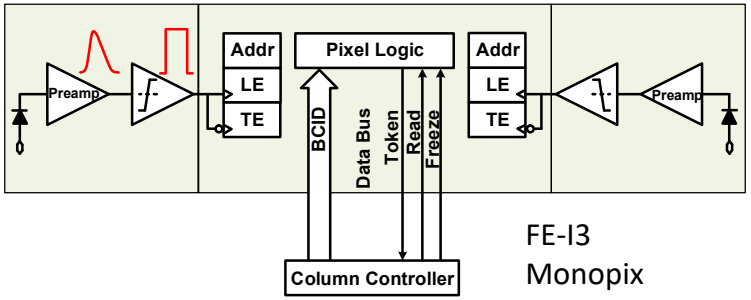
Malta

## One to one



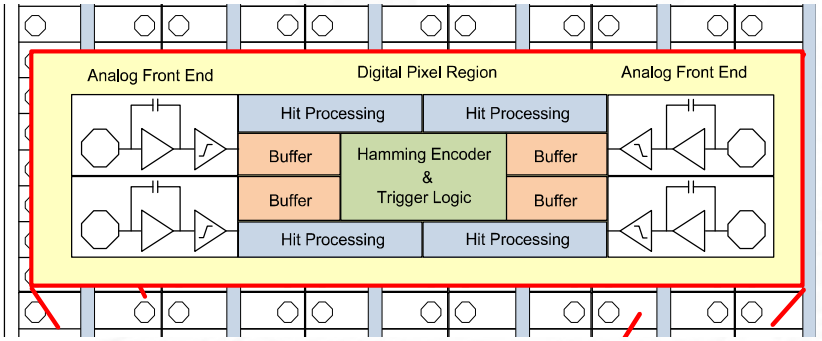

muPix
AtlasPix

## Column-drain



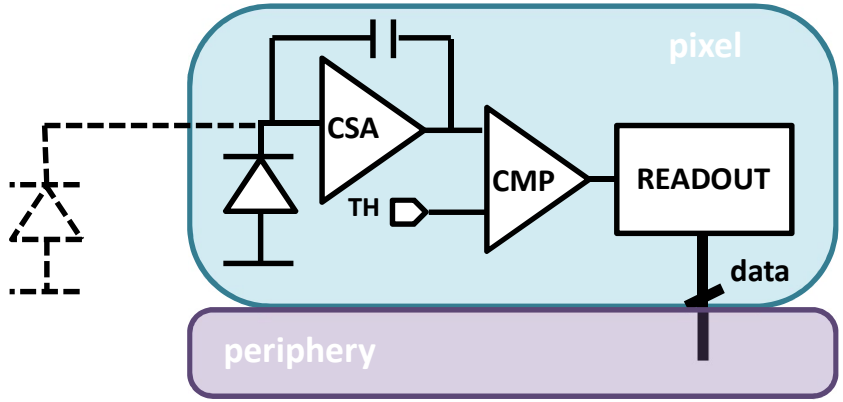

FE-I3
Monopix

## Distributed memory

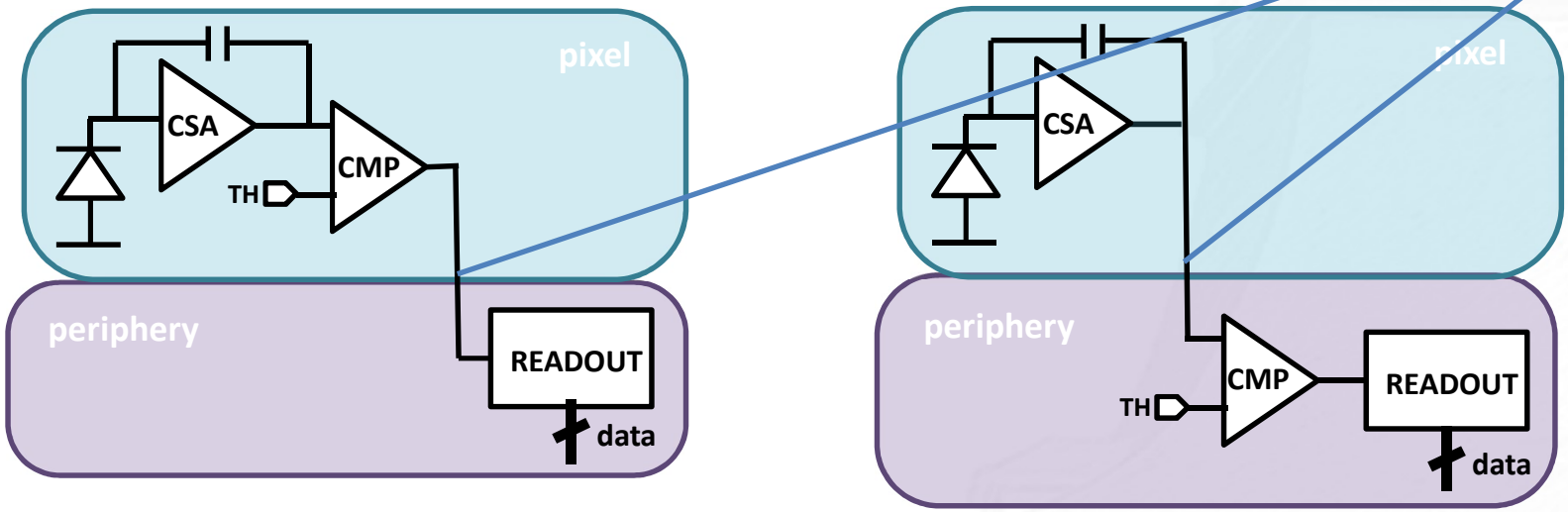



FE-I4
RD53

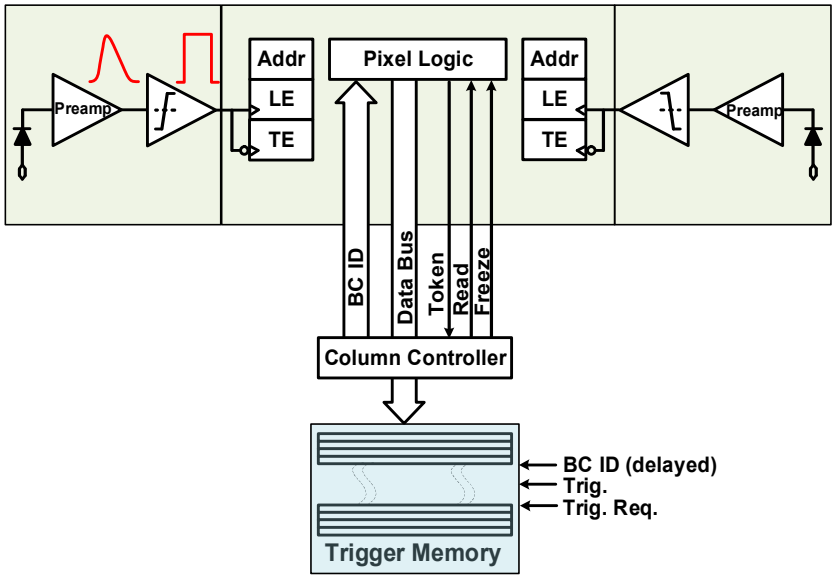
# Readout concepts

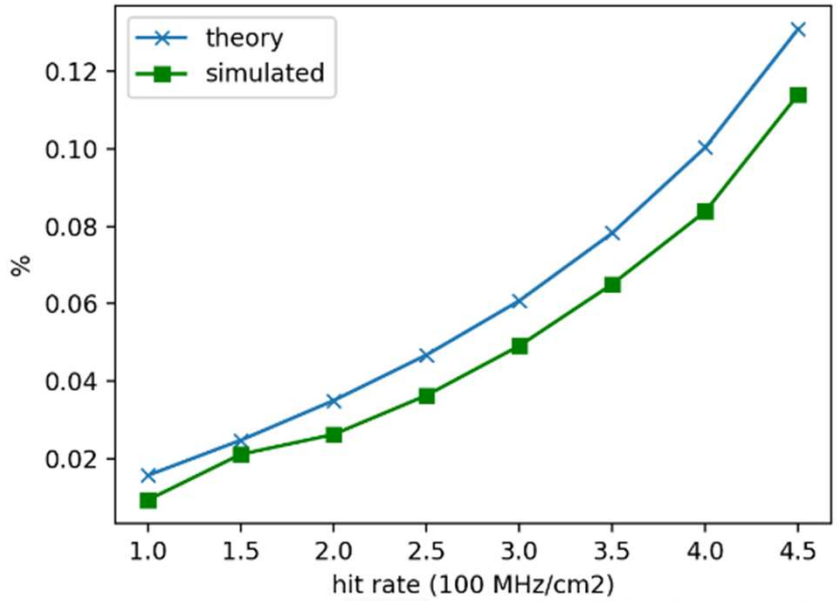



- Lower input capacitance and reduced crosstalk noise
- Overcome limitations of some technologies
- Higher integration level (“3D”)



# Column Drain Architecture

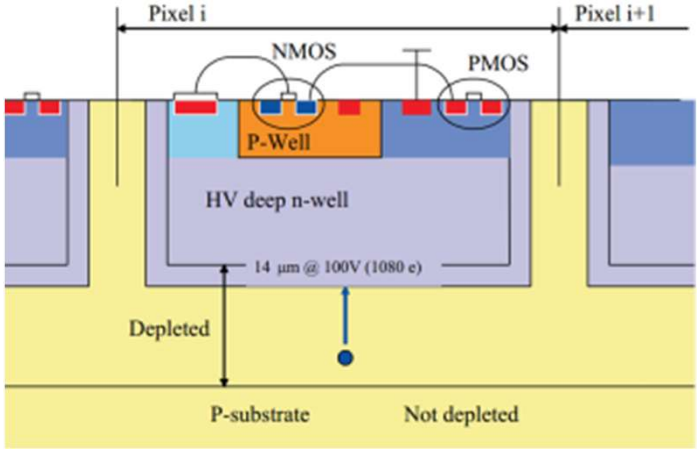


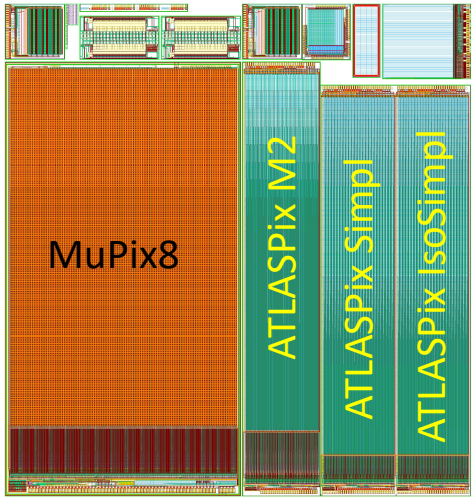

random hit rates for 40x40 μm$^2$ pixels

# Devices & Performance

# HVCMOS - AMS/TSI 180nm

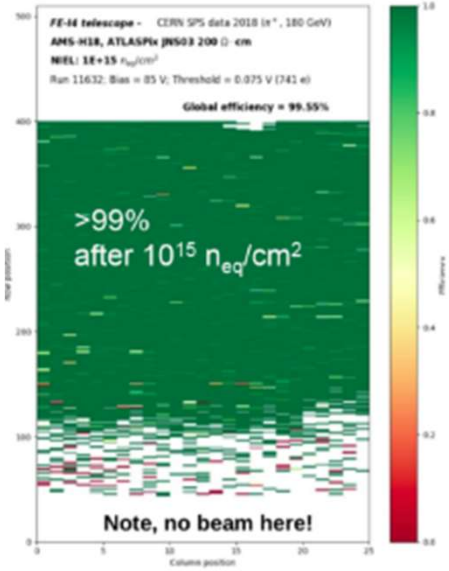


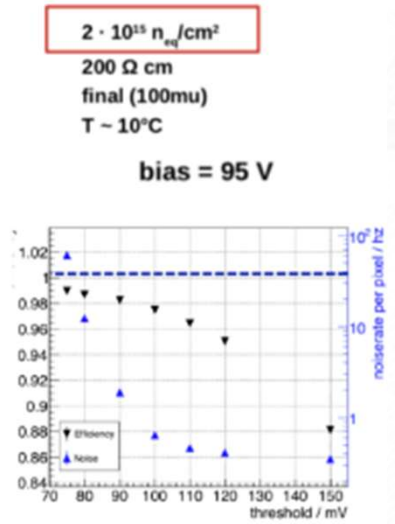

- Substrate: 10 (initially) – 2k Ohm-cm
- Bias: >60 – 100 V
- Process: 180nm
- 3-6 metal layers
- KIT, Geneva, Barcelona, Liverpool, CCPM, CERN, Bonn , ..
- Since 2012




**ATLASPix1 M2**
- 320 × 56 pixel matrix
- 50 × 60 µm² pixel size
- triggered readout

**ATLASPix1 Simple**
- 400 × 25 pixel matrix
- 40 × 130 µm² pixel size

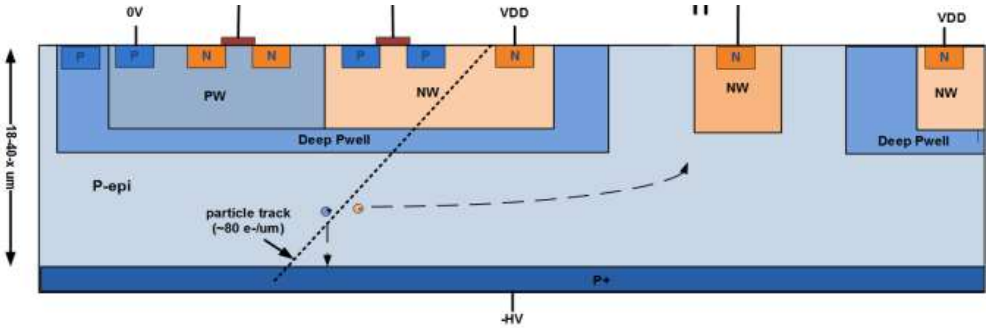



*I. Perić, et al., DOI: 10.1016/j.nima.2018.06.060*
*M. Kiehn, et al.,DOI: 10.1016/j.nima.2018.07.061*

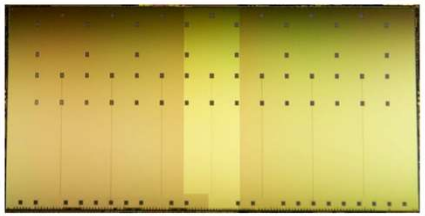
*A.Schoening*

# TowerJazz 180nm

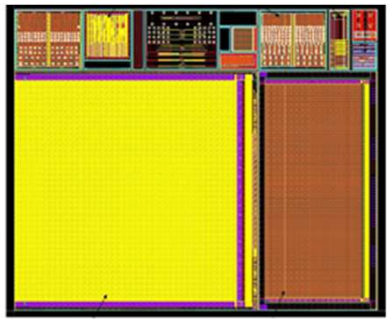



*C. Gao et al., NIM A (2016) 831*
*W. Snoeys et al. DOI:10.1016/j.nima.2017.07.046*

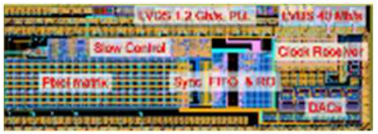
- **TowerJazz** 180 nm CMOS CIS
- Deep Pwell allows full CMOS in pixel
- Gate oxide 3 nm good for TID
- Thickness: 18 – 40 µm
- High resistivity: 1 – 8 k Ohm-cm
- Reverse substrate bias
- **Modified process** to improve lateral depletion
- Derived from ALICE development (CERN)



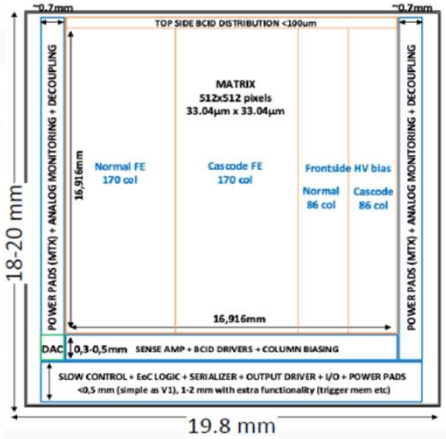
**ALPIDE [ALICE ITS]**
**(x - 2016)**



**TJ-MonoPix/Malta**
**(2018)**

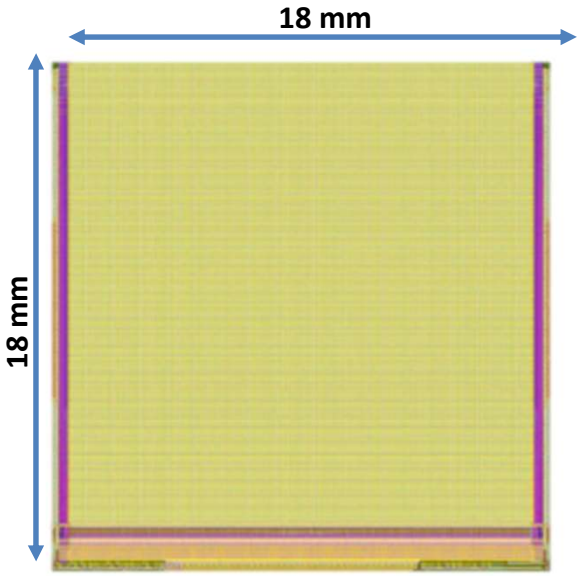



**MiniMalta (2018)**



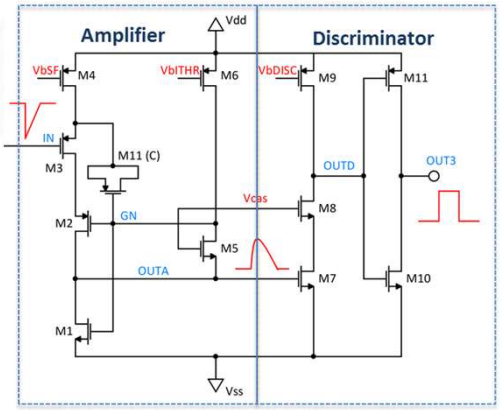

**TJ-MonoPix2 (Q1 2020)**

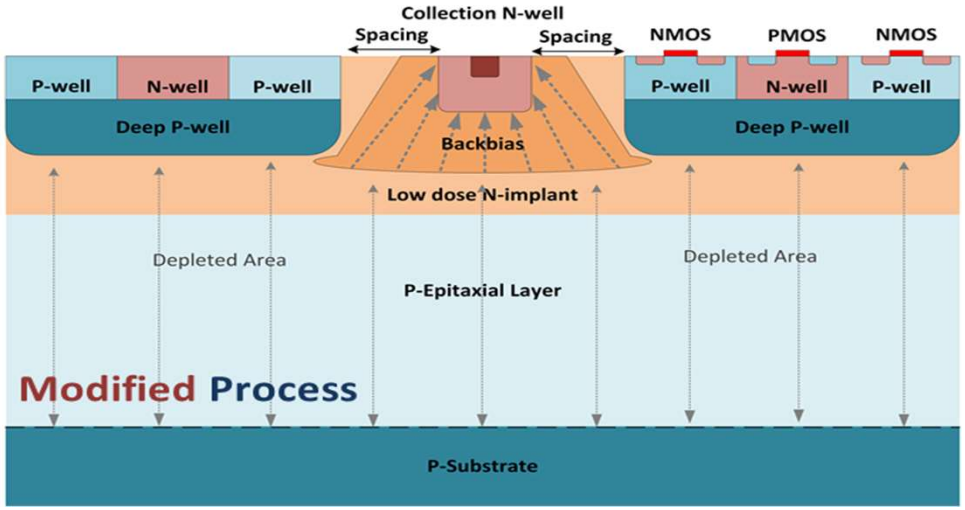
# Malta

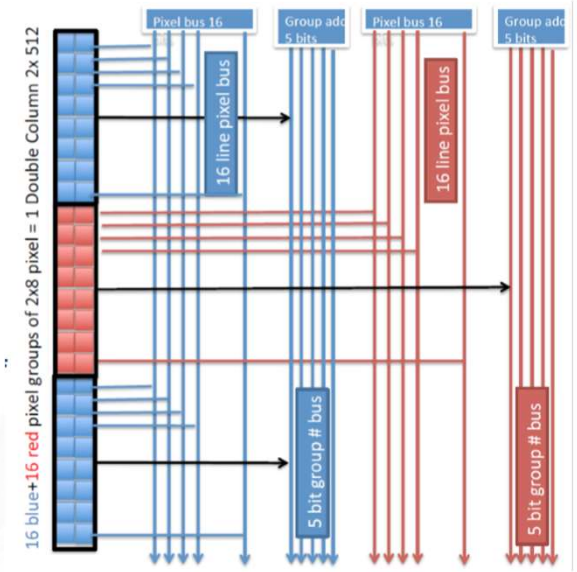



**TJ-MALTA**

- 512x512 pixels (**36.4 x 36.4** µm$^2$ pixel size)
- Design: CERN
- Active area 18 x 18 mm$^2$
- Hit memory in active matrix
- All hits are asynchronously transmitted to EoC logic
- No clock distribution over active matrix



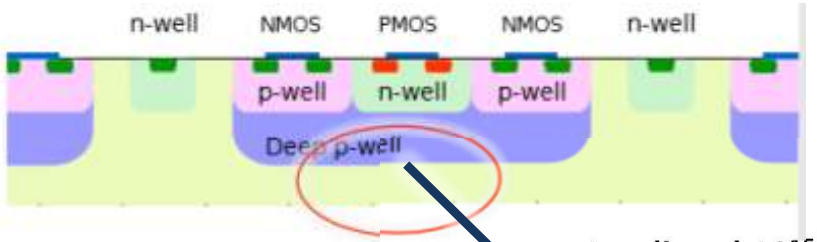



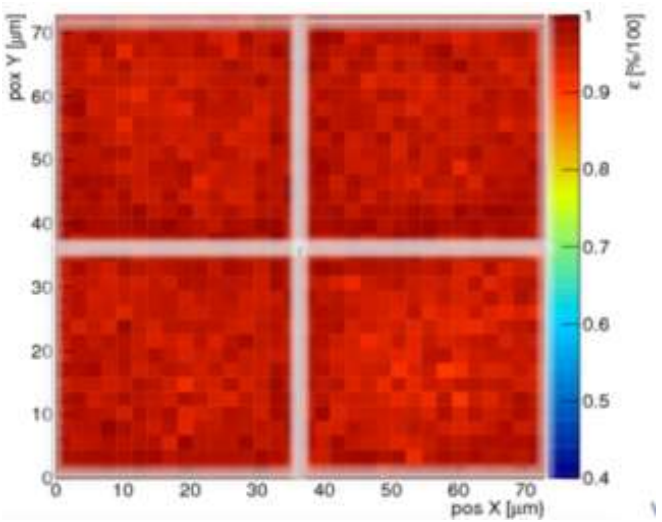

*I. Berdalovic, et. al,DOI: 10.1088/1748-0221/13/01/C01023*

# TowerJazz – Malta Efficiency

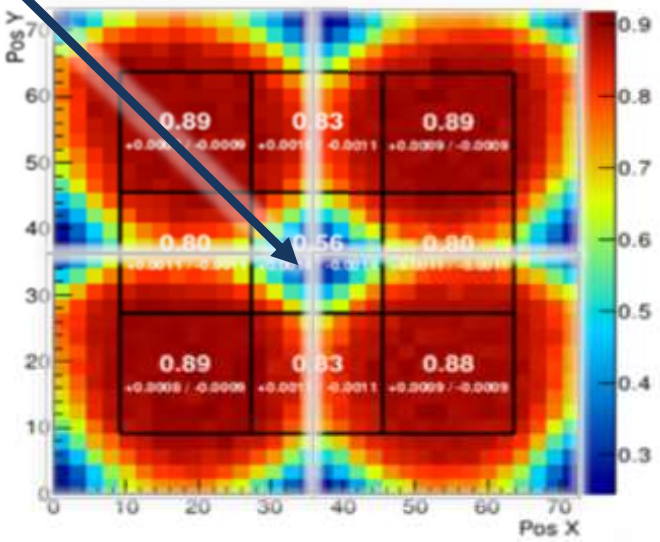
- Due to small collection electrode, the field configuration and charge collection under DPW in pixel corner is critical
- Require full depletion under the DPW
- Transversal field components in corner is needed for radiation hardness




**Unirradiated @ 250e- threshold**

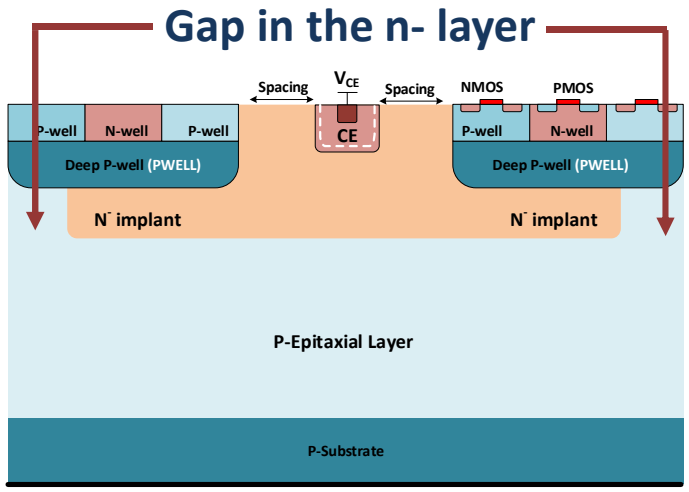


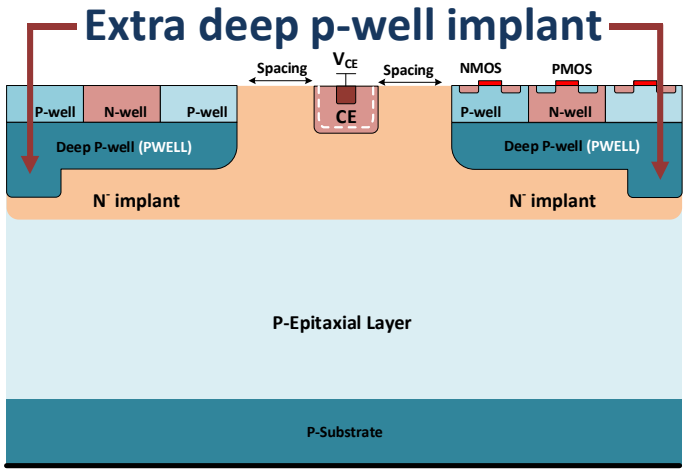

**Irradiated $10^{15}$n/cm2 @ 350e-**

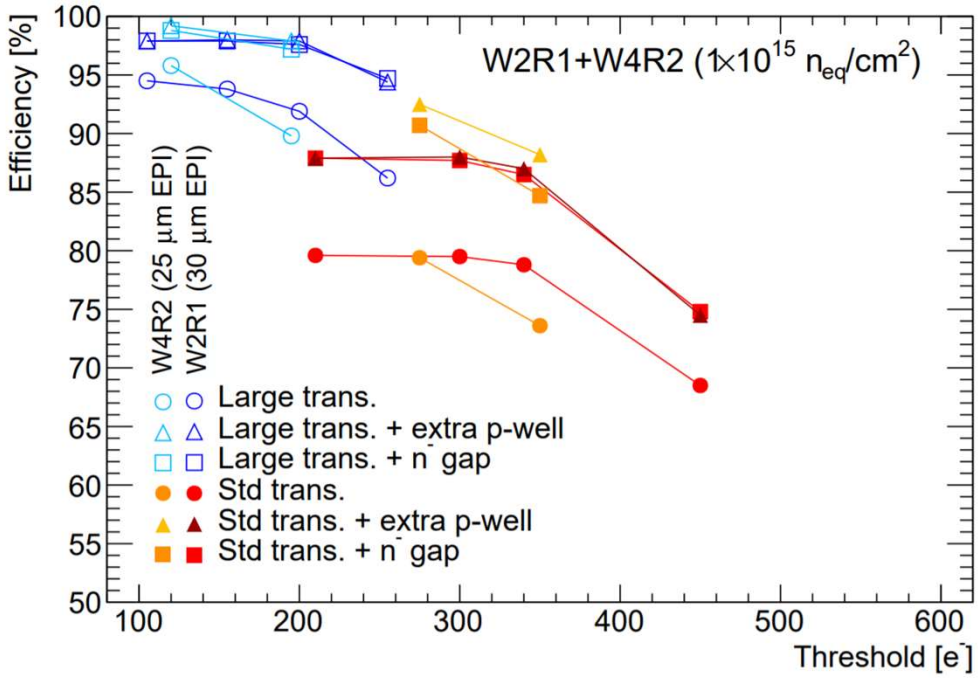



*A. Sharma, et al., Vertex 2018*

# MiniMalta Results



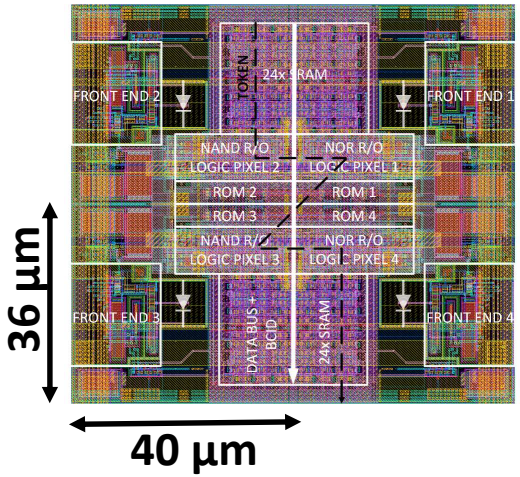



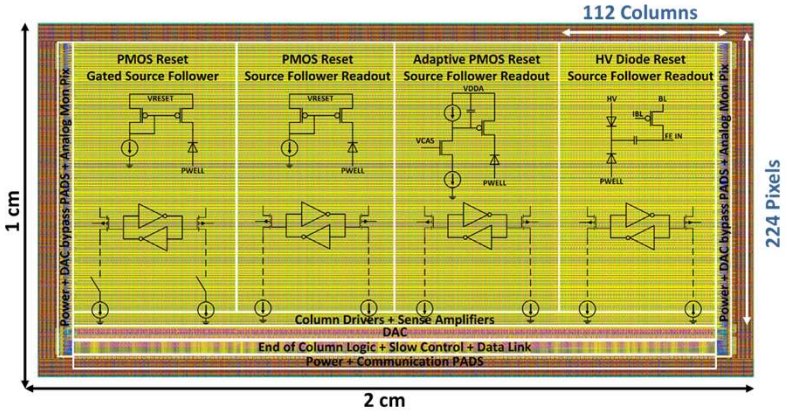




*M. Dyndal arXiv:1909.11987*

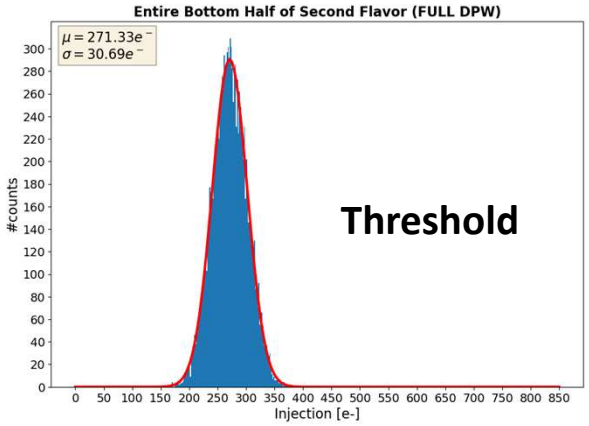
# TJ-MonoPix1

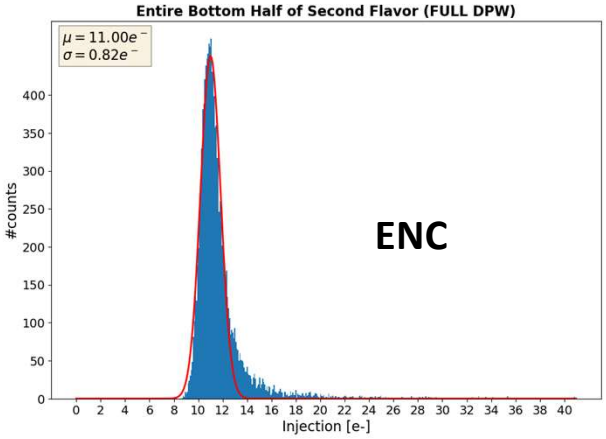
## 2x2 Pixel Layout

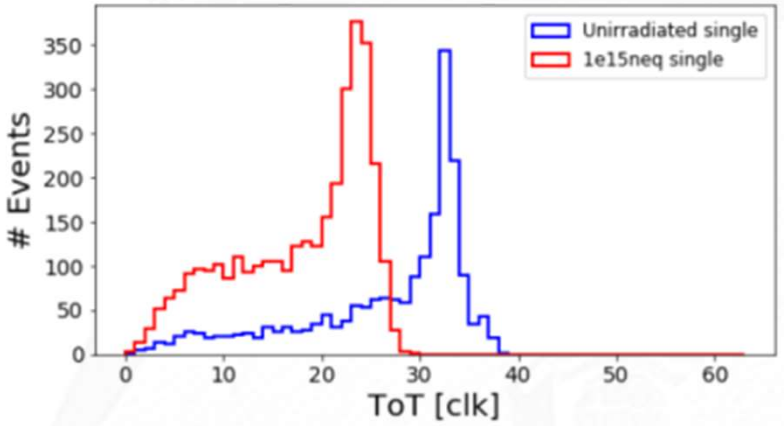



- 1x2cm$^2$ size, 224x448 pixel matrix
- Small pixel size: 36x40 µm$^2$
- Low power: $< 65\ mW/cm^2$
- 6-bit ToA (Time-of-arrival), ToT (Time-over-threshold)
- No trigger memory, 4x40Mhz data transmission
- Optional HV frontside bias, Leakage compensation
- No in-pixel threshold tuning



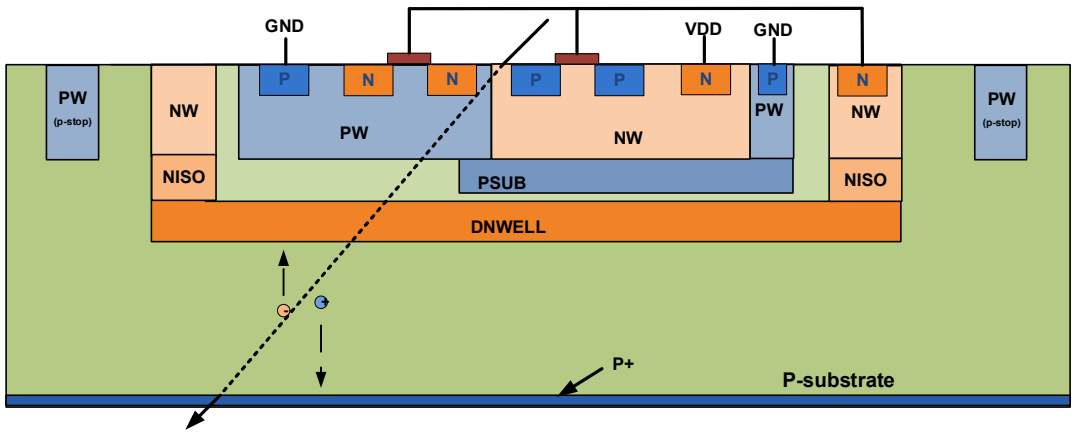





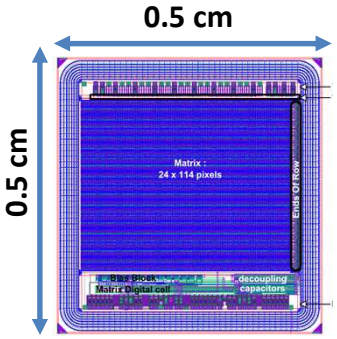
*T. Wang, et al., DOI: 10.1088/1748-0221/13/03/C03039*
*K. Moustakas et al., DOI: doi.org/10.1016/j.nima.2018.09.100*
*I. Caicedo et. al, DOI: 10.1088/1748-0221/14/06/C06006*

# LFoundry LF150

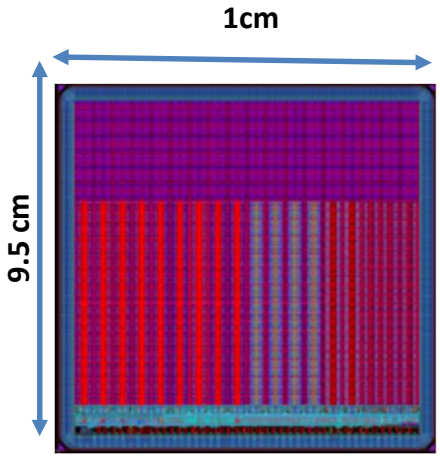



**LFA150:**

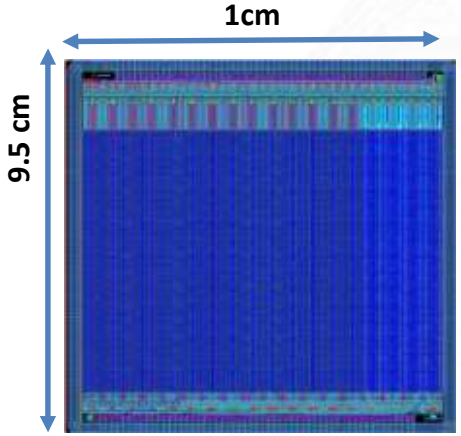
- L-Foundry 150 nm process (deep N-well/P-well)
- Up to 7 metal layers
- **Resistivity of wafer: >2000 Ω·cm**
- Small implant customization
- Backside processing



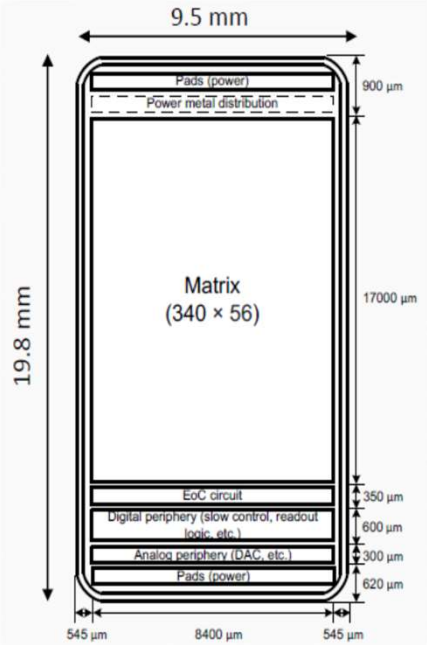

**CCPD_LF**
**2014**




**LF-CPIX**
**2016**

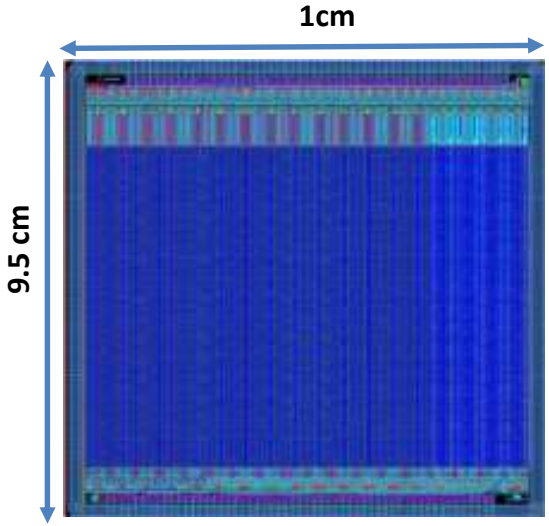



**LF-Monopix**
**2016**



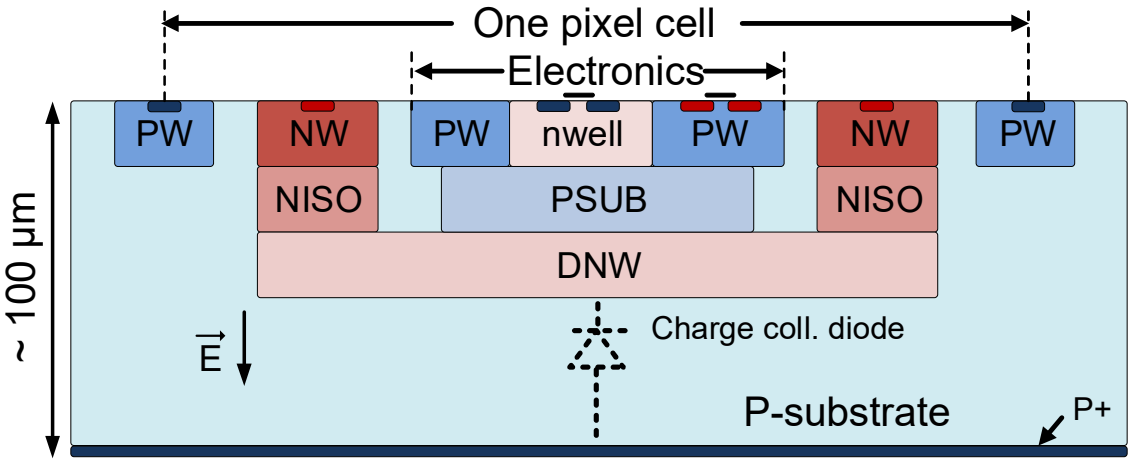

**LF- MonoPix2**
**2020**

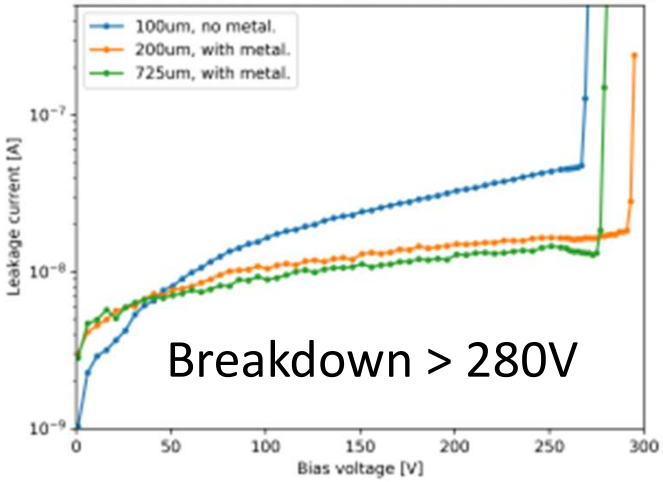
# LF-MonoPix1




**LF-Monopix (monolitic FE-I4)**

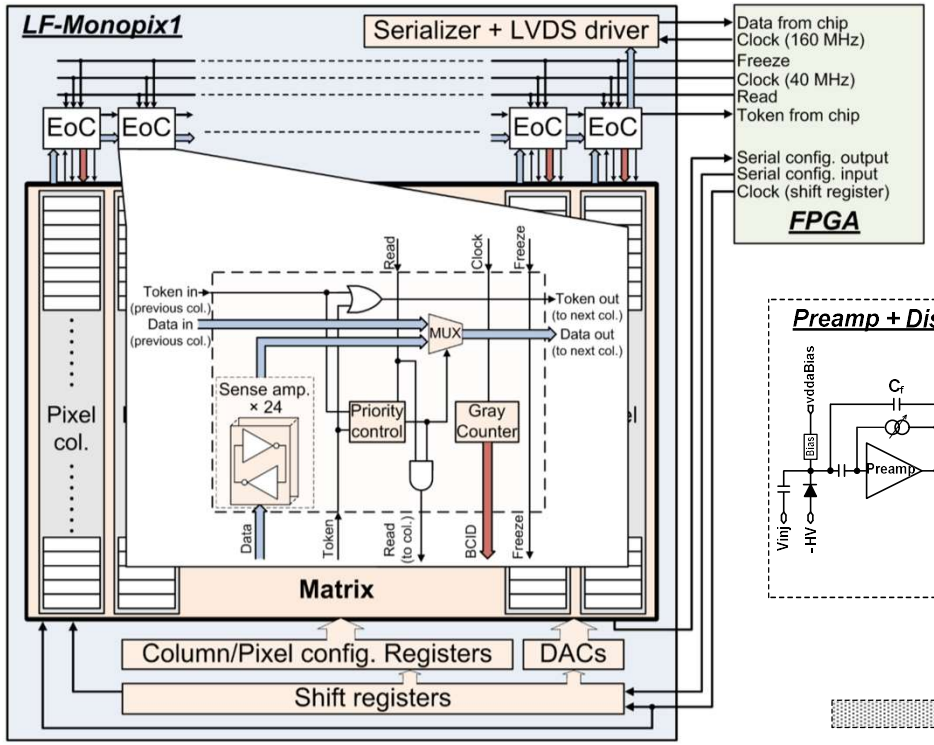
- Pixel size: 50 µm x 250 µm$^2$
- Chip size: 10 mm x 10 mm$^2$
- **200µm and 100µm version**
- Measured good >99% particle (MIP) detection after high neutron radaition
- Breakdown >280V on test structures
- Radiation (TID) tolerance (>0.50MGray)
- **LF-MonoPix2 -> (150x50µm$^2$)**



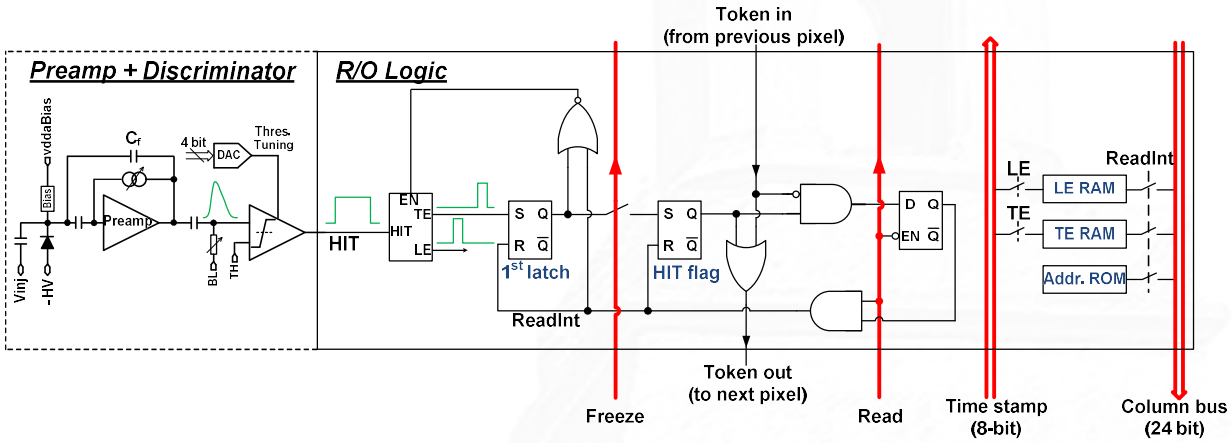



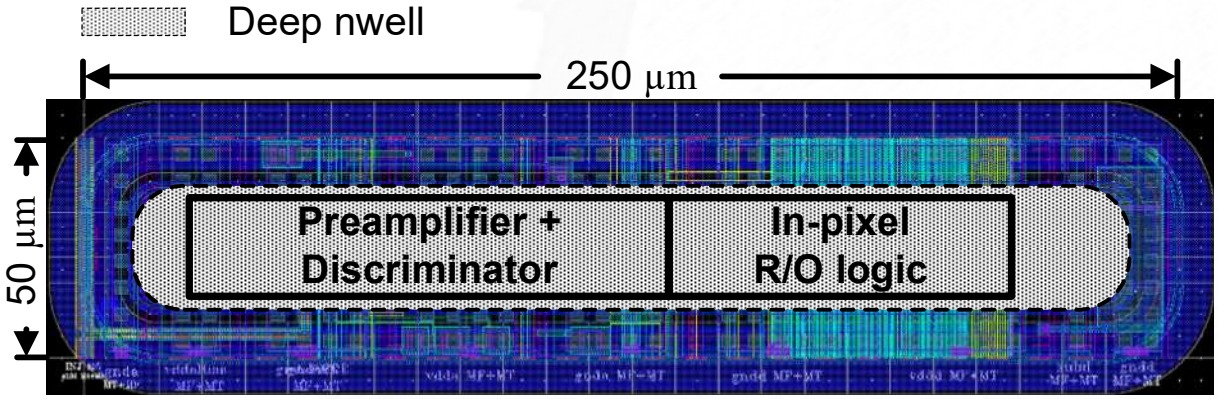

*M. Barbero, et al., "Radiation hard DMAPS … „ arXiv:1911.01119*

# LF-MonoPix1 Design




- Pixel size 50 × 250 µm²





*T. Wang, et al., DOI: 10.1088/1748-0221/12/01/C01039*
*P. Rymaszewski et al., DOI: http://doi.org/10.22323/1.313.0045*

# LF-MonoPix1 Measurements

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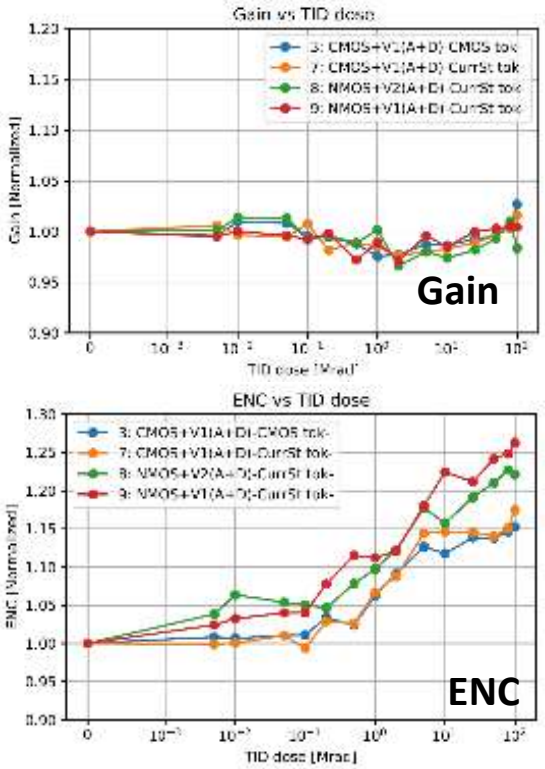
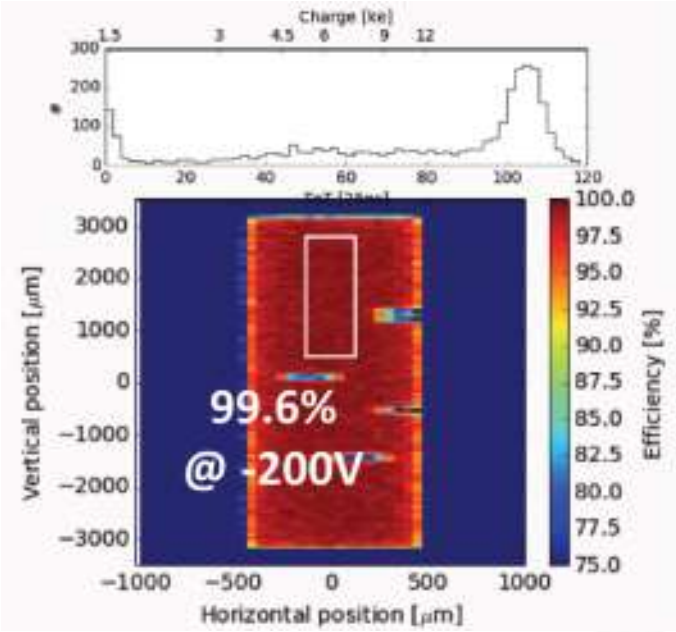
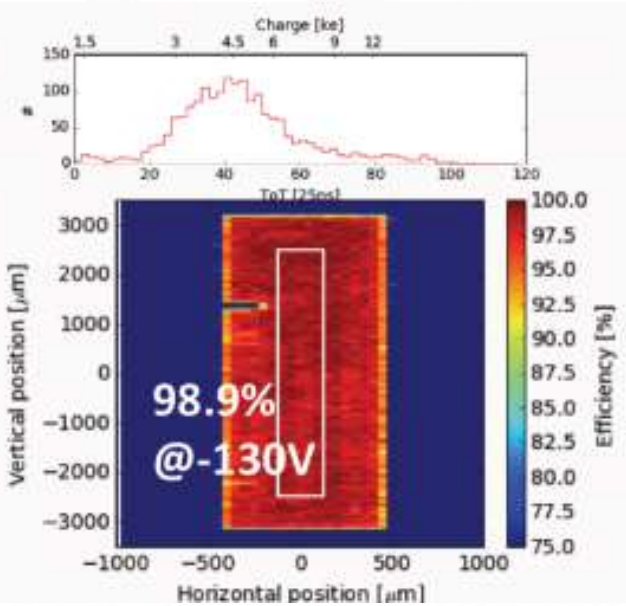
## TID Effects




## Efficiency (Un-irradiated)

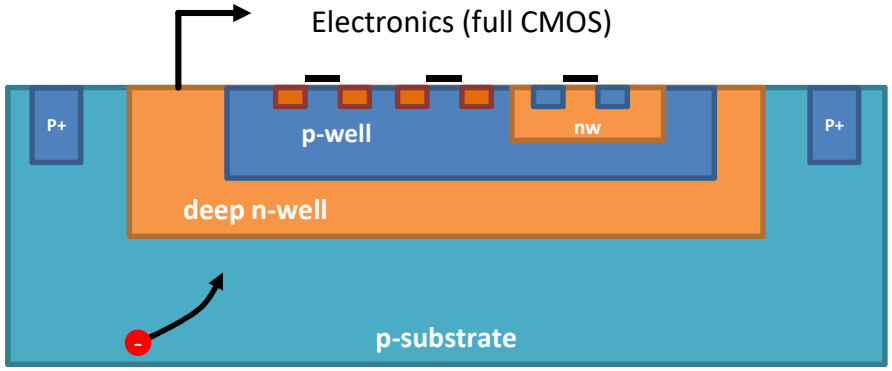


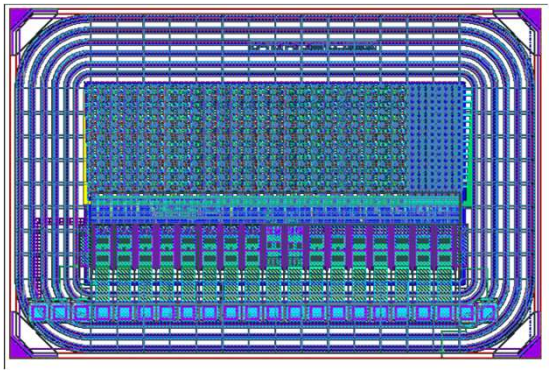

## Efficiency (1 x $10^{15}$ $n_{eq}/cm^2$)



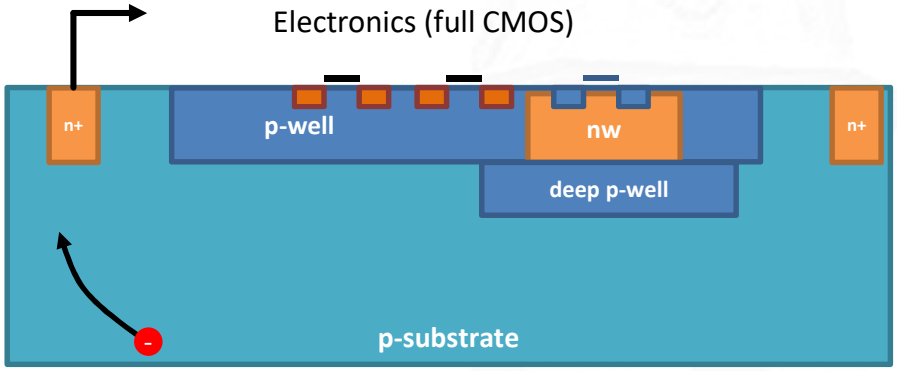

*T. Hirono, et. al, DOI: 10.1016/j.nima.2018.10.059*

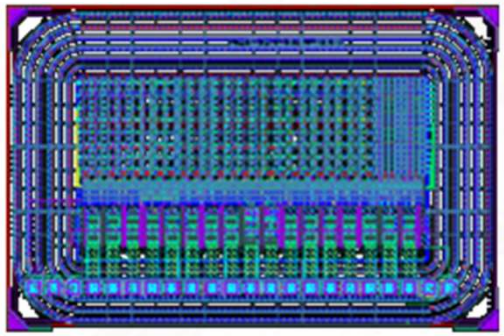
# Other LFoundry Development



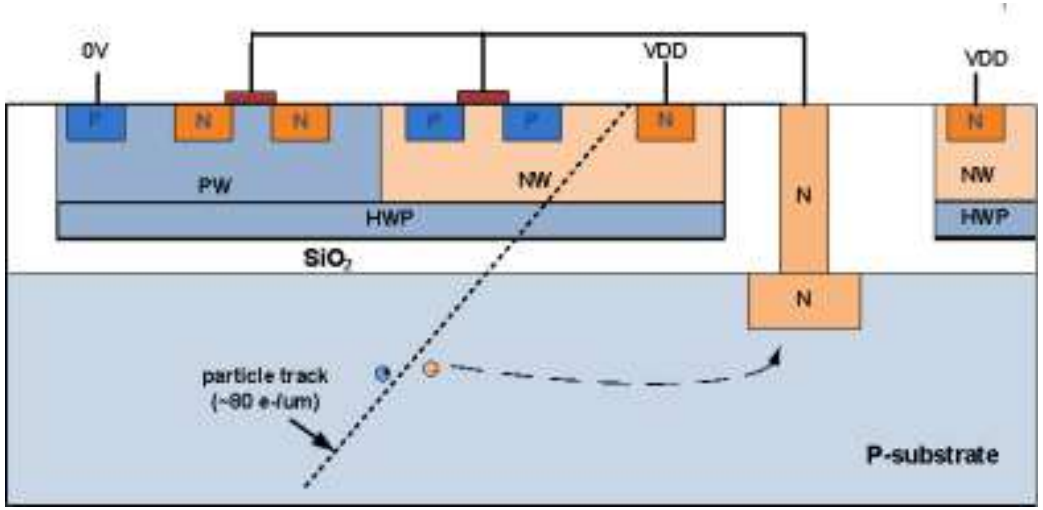
- Architecture: 3T (DC coupled)
- **Thickness: 100 and 200µm (BSI)**
- **Bias: < 250V**
- Pixel: **25x25µm²**
- Input capacitance:  tens od fF



- Architecture: 3T (DC coupled)
- **Thicknes: 100 and 200µm(BSI)**
- **Bias: < 60V**
- Pixel: **25x25µm²**
- Input capacitance**: few fF**

# X-FAB HV-SOI (XT180)

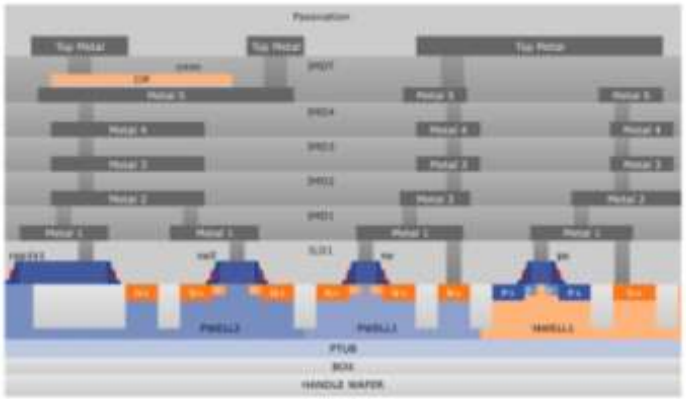


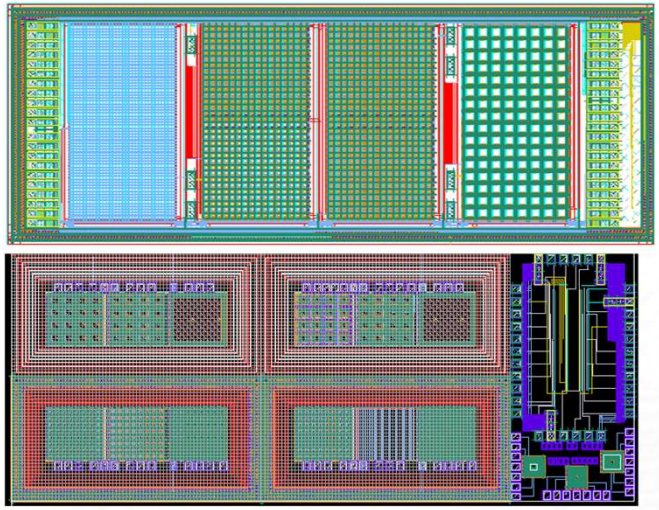

**XT180:**

- XFab 180 nm HV-SOI
- Up to 7 metal layers
- Resistivity of wafer: 100 Ω·cm

**XTB01 and XT02 prototypes:**

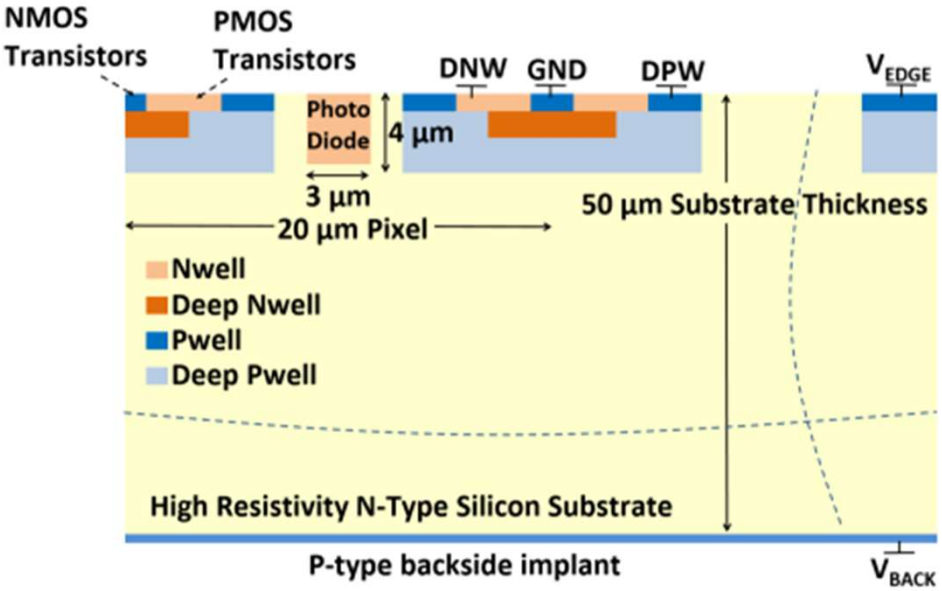
- Pixel pitch: 15, 50, 100 µm
- Chip size: 2.5 mm x 5 mm
- Design/Testing: Bonn, CERN, CPPM





*Fernandez-Perez et al. NIM A796 (2015) 13-18*
*Hemperek et al. JINST 10 (2015) no.03, C03047*

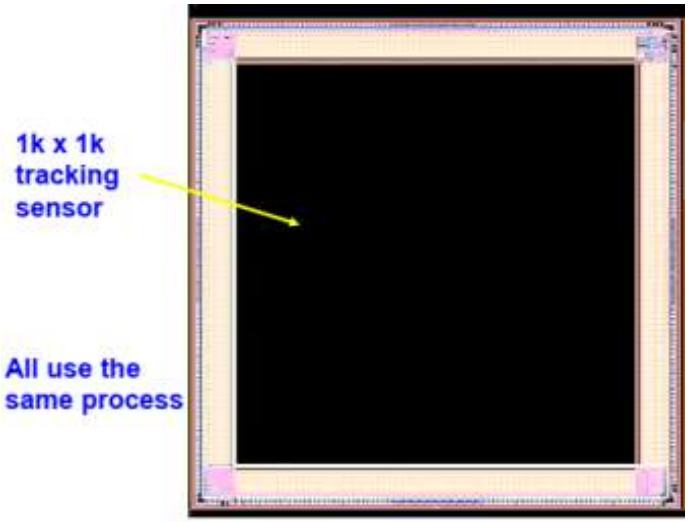
# Deep Depletion CMOS

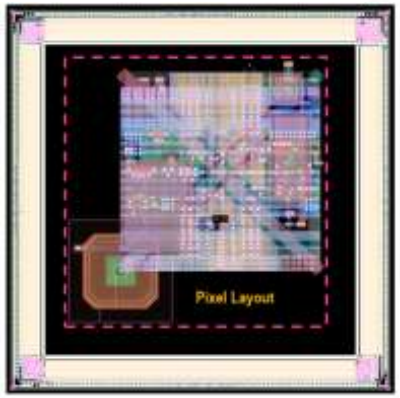



Sensor Creations

**CMOS Process on High Resistivity Silicon**

- Technology node: 180nm
- Wafer material: 8 inch float zone (FZ)
- Resistivity: 6.5 kOhm x cm
- Conductivity type: N
- Backside: P+ implant with dedicated electrode
- Thickness: 50 – 400 micron (application specific)



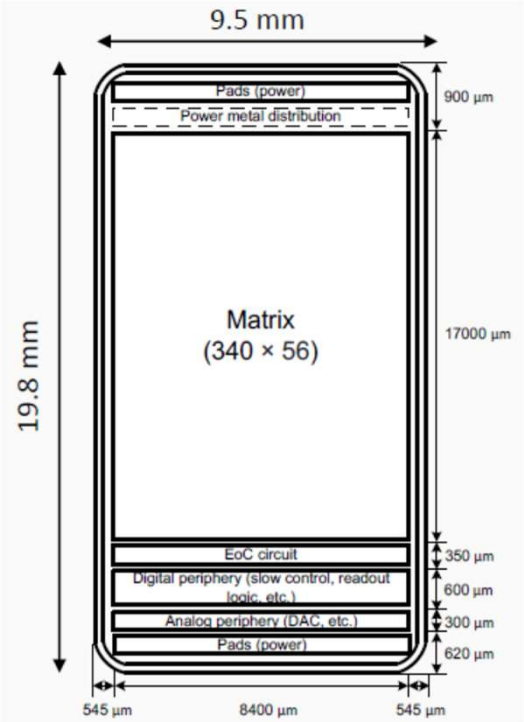

- **25 x 25 mm² overall size**
- **1024 x 1024 pixels**
- **20 µm pixel size**
- **Four-fold symmetric**
- **All available 6 metal layers used for power routing**

*S. Lauxtermann, "Monolithic Deep Depletion CMOS Pixel ...", Pixel2018*

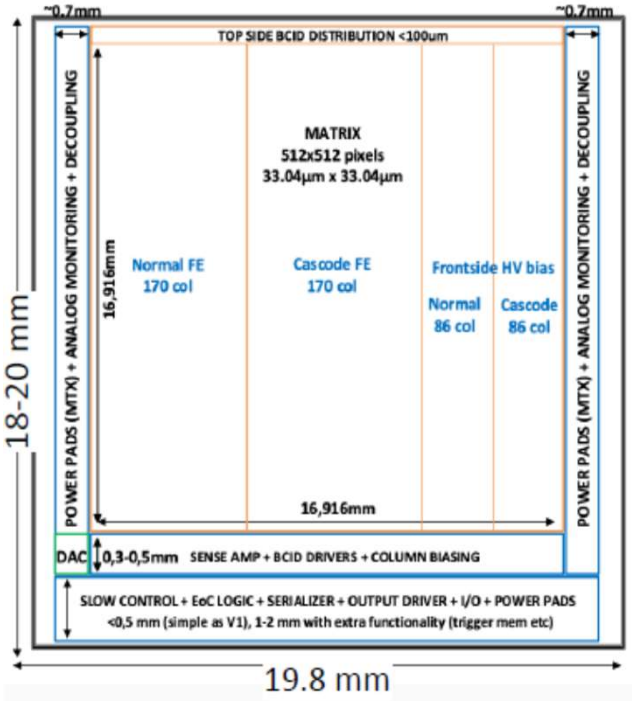
# Future

# MonoPix2

## LF-MonoPix2




## TJ-MonoPix2



# Power estimates

LF-MonoPix : ~300mW/cm2 (~20% digital)

TJ-Monopix : ~150mW/cm2 (~50% digital)

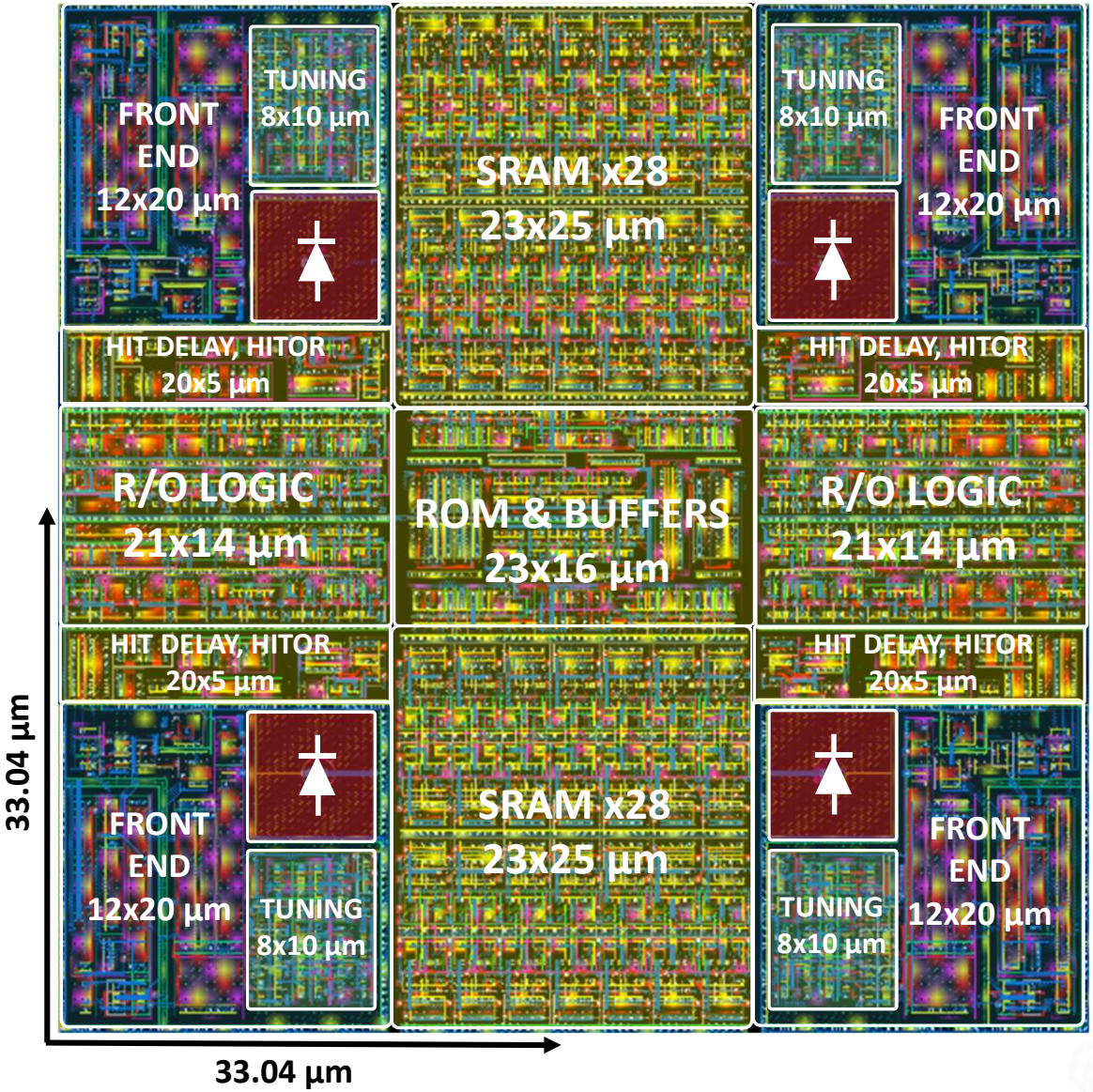
TJ-Malta : ~110mW/cm2 (~25% digital)

Remainder: for timing resolution of **25ns**

**Analog**: ~scales with **bandwidth** (time resolution) and input capacitance
(does not scale with technology easily)

**Digital**: ~scales with **timing resolution and hit rate**
(large gain from technology scaling)

# TJ-Monopix2 scaling




**Process 180nm (25ns, >100MHz/cm$^2$):**

Does not scale with technology:

- Diode : ~64µm$^2$
- Front-End : ~240µm$^2$

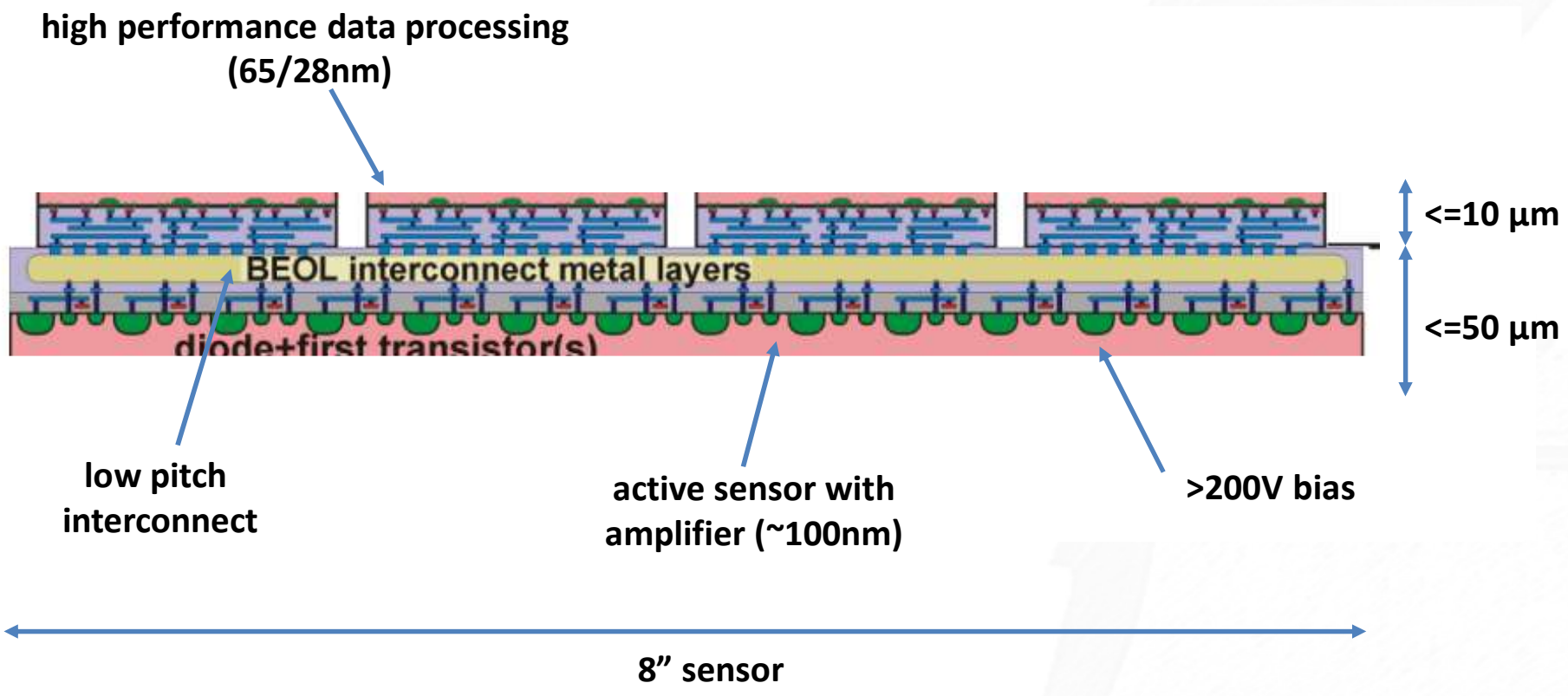
Scales with technology:

- SRAM: 575µm$^2$
- Tuning: 80µm$^2$
- R/O Logic: 294µm$^2$
- HitOr:100µm$^2$
- ROM & Buffers: 368µm$^2$

From 180 to 65nm*
(digital scales ~x8-10):
$\Rightarrow$ ~ 20x20µm$^2$

drop analog information?
more signal => simpler amplifier
less hit rate => simpler logic

# Ultimate detector platform?




**“Easily” available today!**

# Some concepts from Belle II

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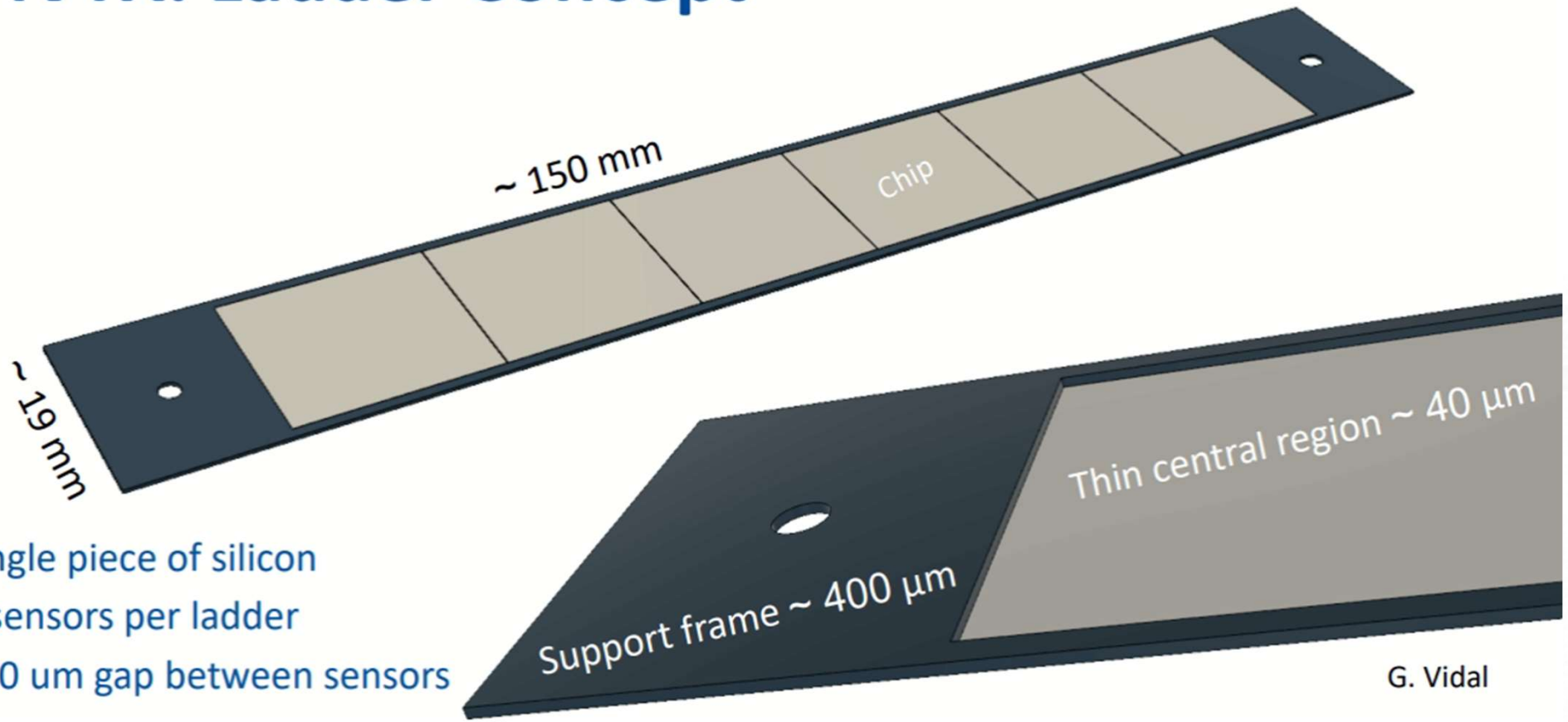
## iVTX: Ladder Concept




Single piece of silicon
6 sensors per ladder
100 um gap between sensors

*C. Marinas , " Belle II VXD Open Workshop" 2019*

# Conclusions

- Proven good radiation tolerance of sensors (and electronics)
- Lower cost alternative to conventional hybrid sensors (as monolithic or cheaper hybrid)
- Limited complexity (110-180nm)
- Successful backside processing 200/100µm (50µm possible)
- Low mass (<50µm)
- Hybridizing active sensor and R/O chip can increase performance of hybrid sensors (wafer to wafer?)

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SI LAB
Silizium Labor Bonn