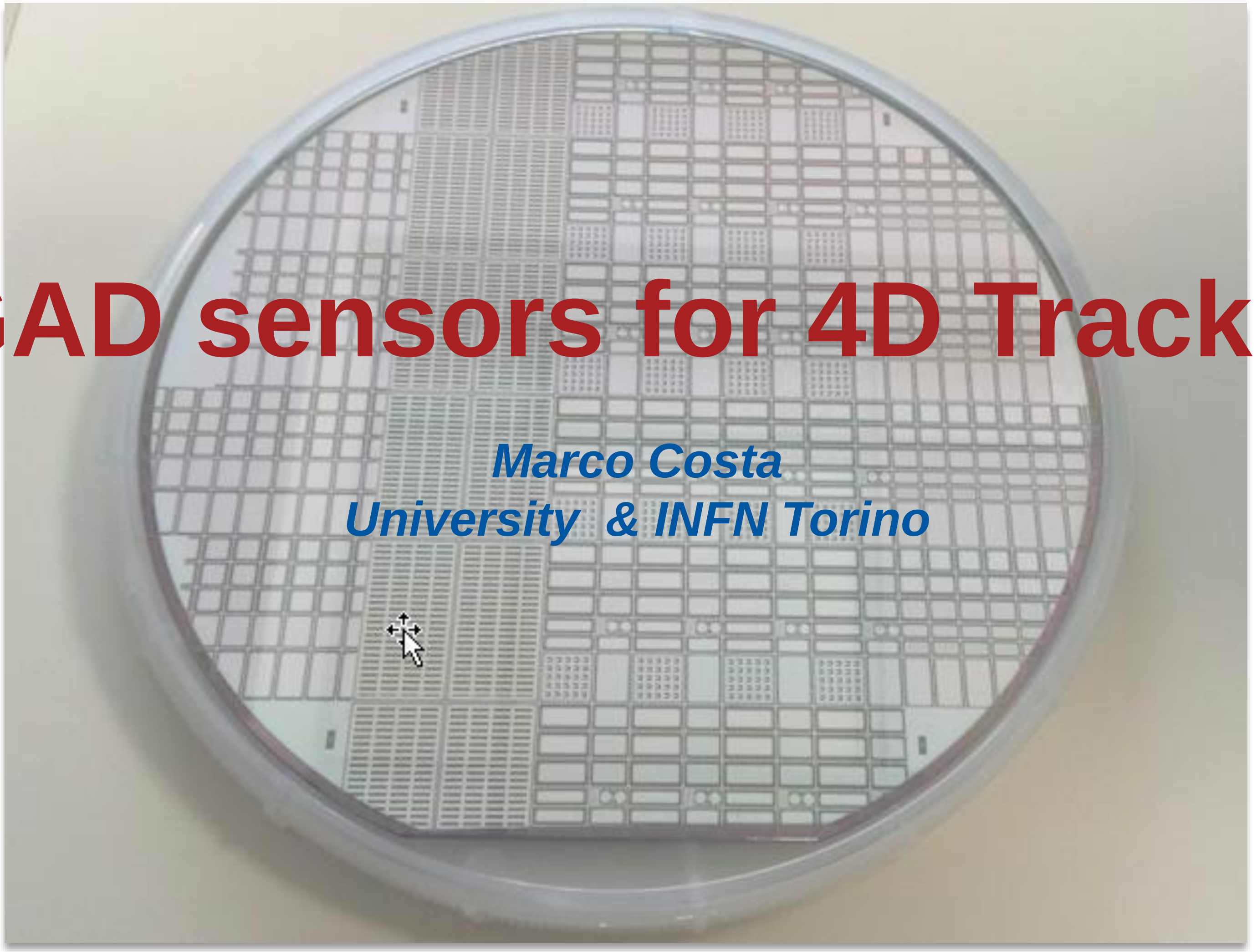
LGAD sensors for 4D Tracking



Marco Costa
University & INFN Torino

Tracking particles in space and time

Particle physics experiments have developed **formidable tracker systems:**

- Many millions of channels
- Extremely good spatial resolution

However,

silicon sensors were never considered as accurate timing devices

the R&D of the last 5-10 years have changed completely the landscape

At present, silicon sensors are the ONLY detector able to provide excellent timing capability (~ 30 ps) , good radiation hardness (fluence ~ 1E15 n/cm2), good pixilation (10um – 1 mm), and large area coverage (many m^2)

Face the challenge by adding Timing information

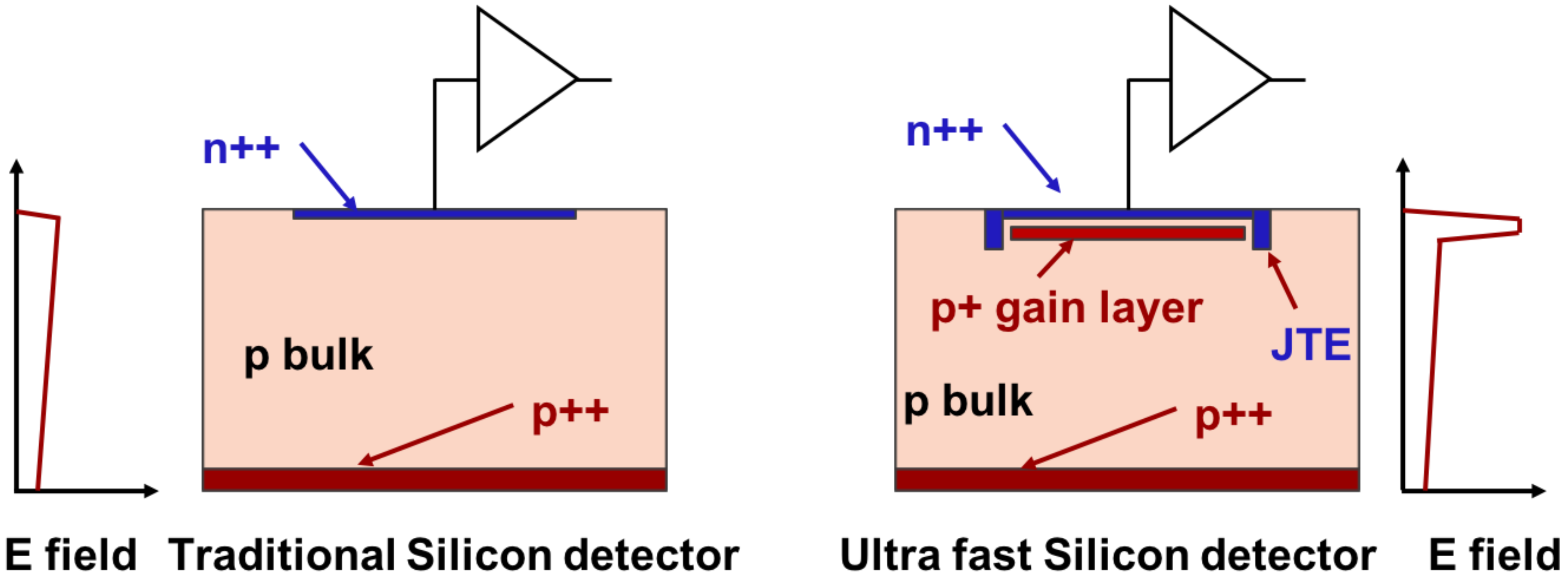
The inclusion of track-timing in the event information has the capability of changing radically how we design experiments.

Timing can be available at different levels of the event reconstruction, in increasing order of complexity:

1) Timing in the event reconstruction ➔ **Timing layers**
   - this is the easiest implementation → CMS, ATLAS
2) Timing at each point along the track ➔ **4D tracking**
   - tracking-timing
3) Timing at each point along the track at high rate ➔ **$4D^+$ tracking**
   - Very high rate represents an additional step in complication, very different read-out chip and data output organization

Ultra Fast Silicon Detectors

Ultra Fast Silicon Detectors (UFSDs) are Low Gain Avalanche Diodes (LGADs) optimized for timing employing a thin multiplication layer to increase the output signal at the passage of a particle of a factor ~10 - 20

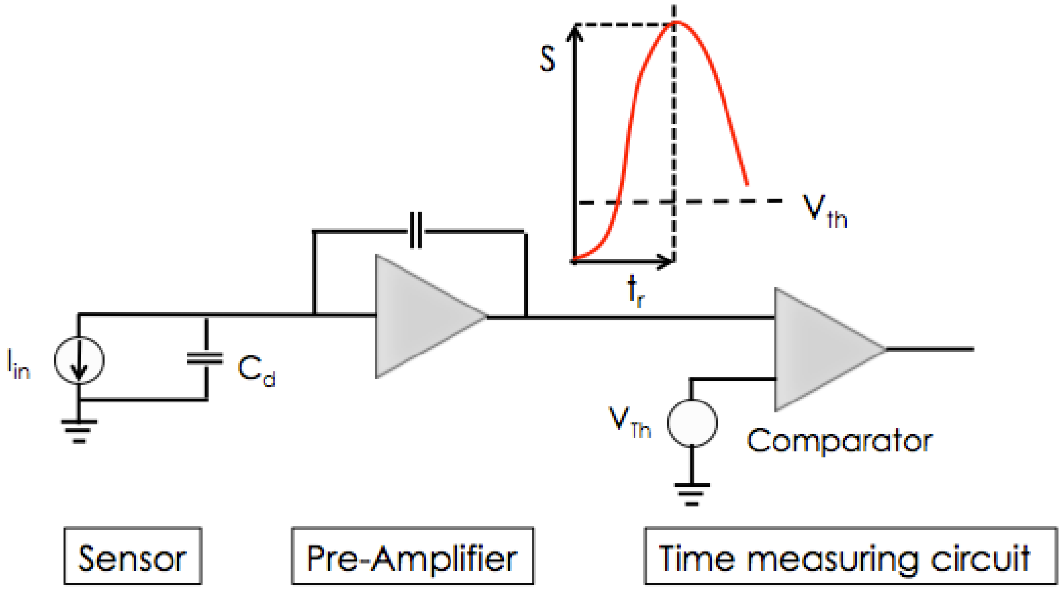


The low-gain mechanism, obtained with a moderately doped p-implant, is the defining feature of the design.

The low gain allows segmenting and keeping the shot noise below the electronic noise, since the leakage current is low.

Silicon time-tagging detector

(a simplified view)



Time is set when the signal crosses the comparator threshold

The timing capabilities are determined by the characteristics of the signal at the output of the pre-Amplifier and by the TDC binning.

Strong interplay between sensor and electronics

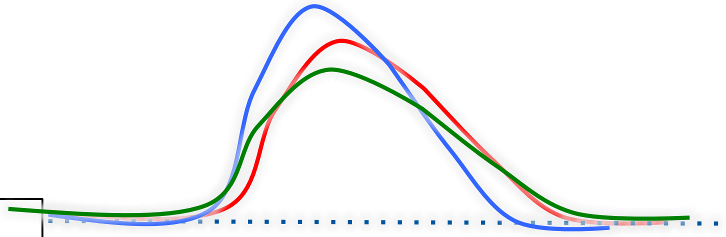
Good time resolution needs very uniform signals

Signal shape is determined by Ramo's Theorem:

$$i \; \mu \; qvE_w$$

Drift velocity

Weighting field



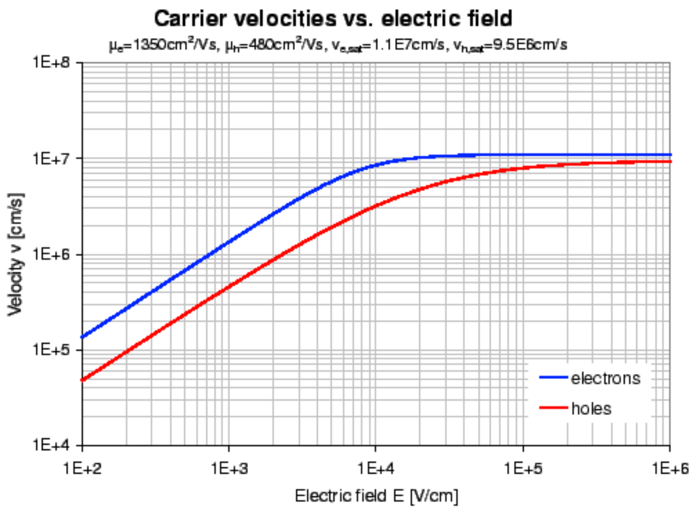
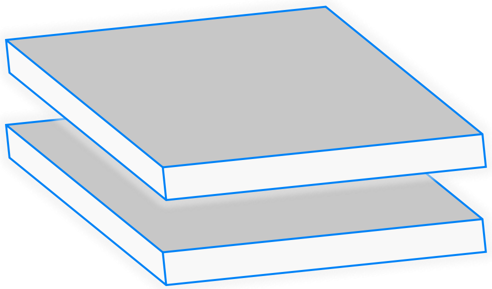


Figure: Electron and hole velocities vs. the electric field strength in silicon.

he key to good timing is the uniformity of signals:

rift velocity and Weighting field need to be as uniform as possible

asic rule: parallel plate geometry

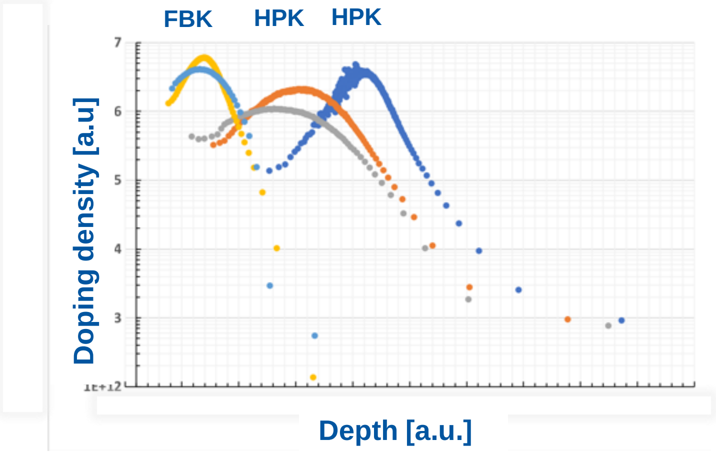


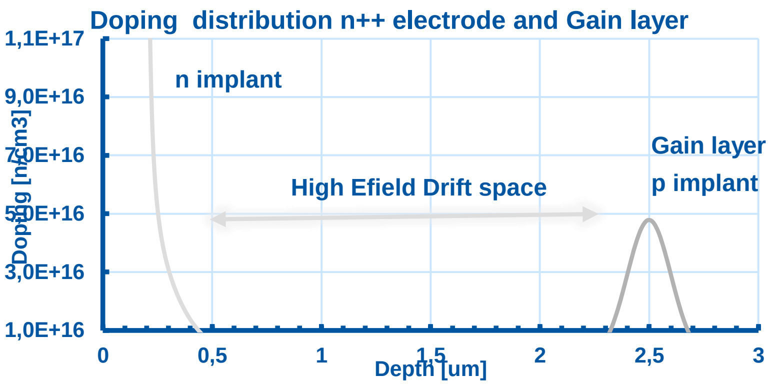
Gain layer: a parallel plate capacitor with high field

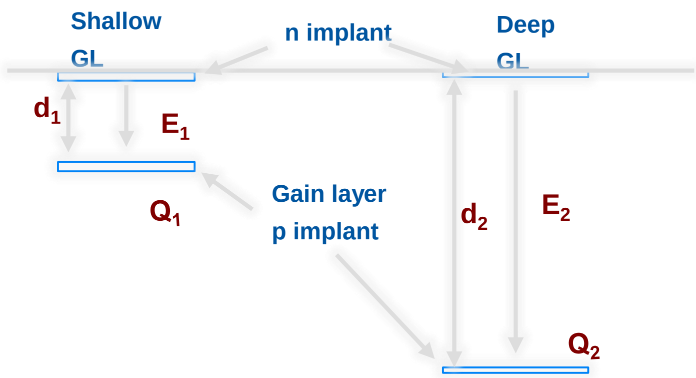
- The doping of the gain layer is equivalent to the charge on the plates of the capacitor.
- Bias adds additional E field

Gain: exp(field * distance) $G \propto e^{\alpha * d}$

Shallow gain layers work at higher E field.







$E_1 > E_2$

- **Examples of gain layer shapes from a few of our samples.**
- **GL differs for depth and width: both parameters are important.**

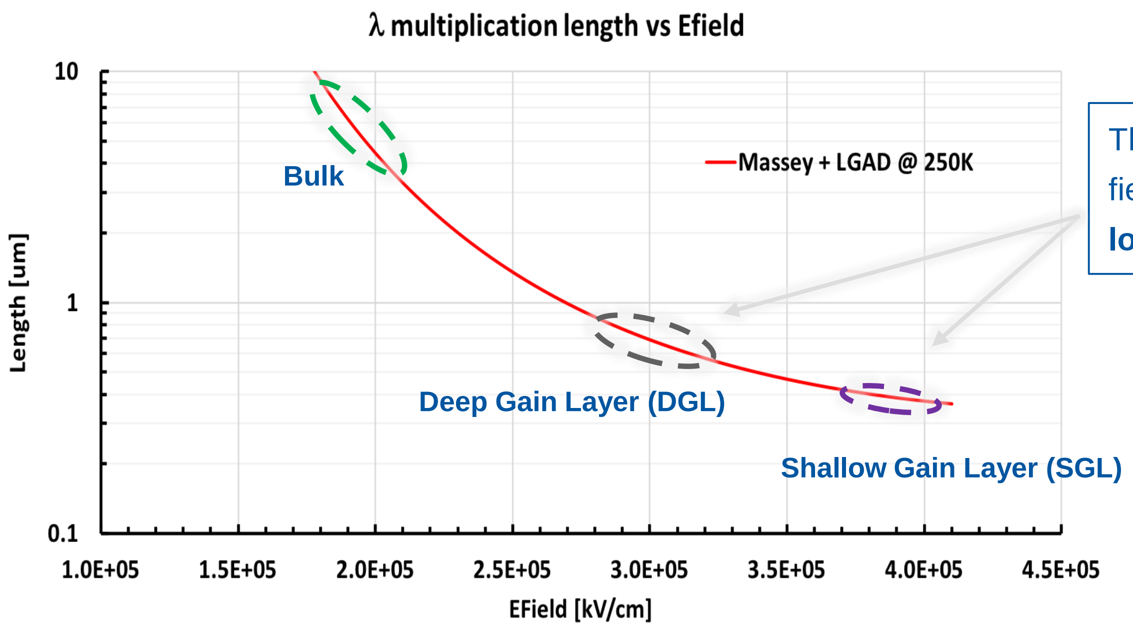
Mean free paths in different situations

1. Multiplication in the Bulk: ~ 170-200 kV/cm
2. Deep Gain Layer: ~ 290 – 300 kV/cm
3. Shallow Gain Layer: ~ 380 – 400 kV/cm

$$G \propto e^{\alpha(E,T)*d}$$

$$\alpha \propto e^{-(a+b*T)/E}$$

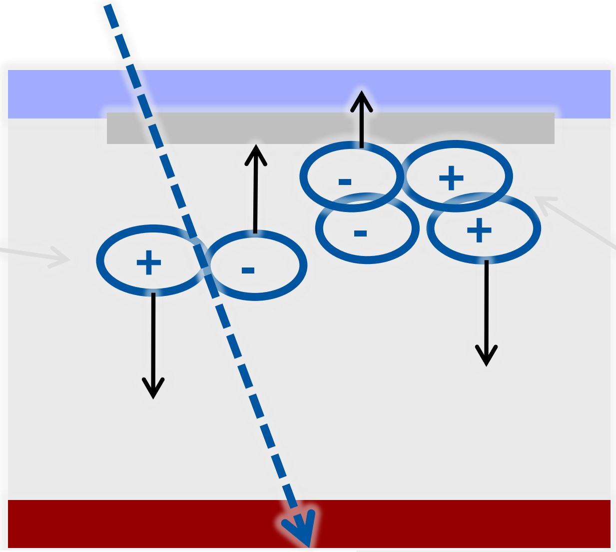
Massey model: $b = \sim 500\ V/K$



The position of the GL determines the field working point: **the deeper it is, the lower the field is**

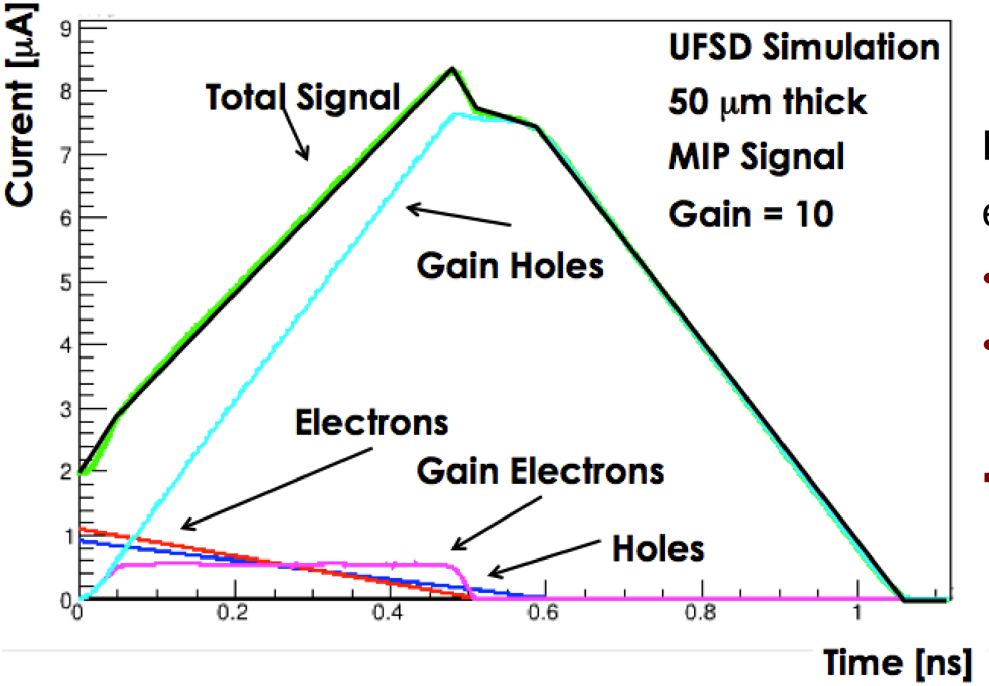
How gain shapes the signal

Initial electron, holes



Gain electron: absorbed immediately

Gain holes: long drift home



Electrons multiply and produce additional electrons and holes.

- **Gain electrons have almost no effect**
- **Gain holes dominate the signal**

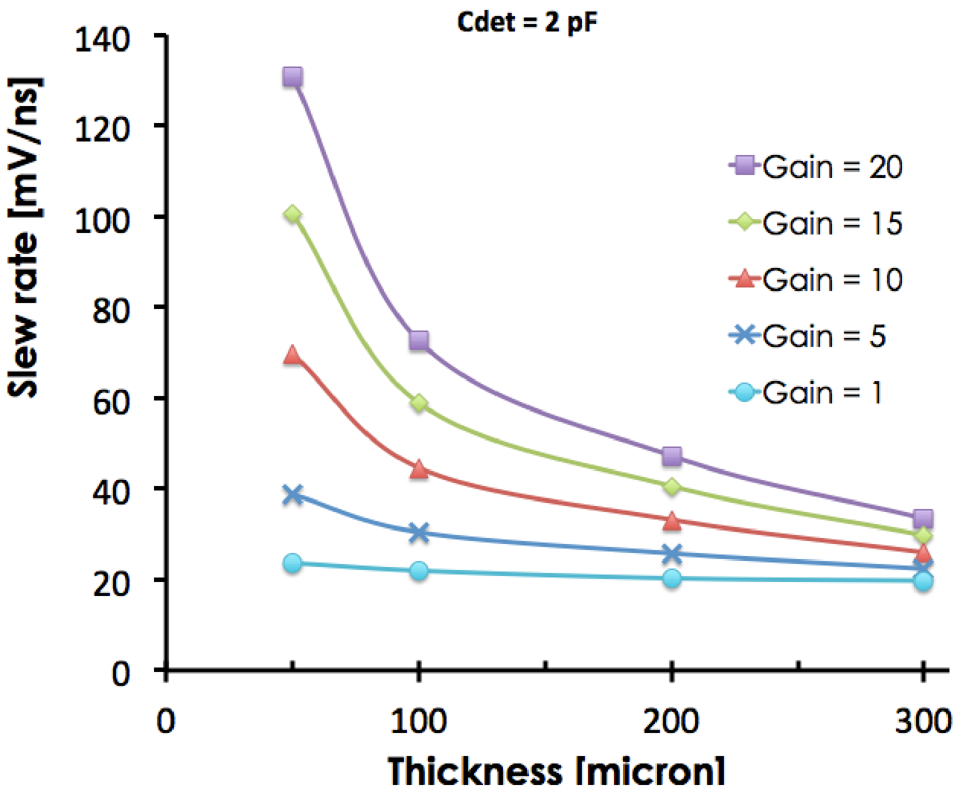
➔ **No holes multiplications**

Gain current vs Initial current

$$\frac{di_{gain}}{i} \propto \frac{dN_{Gain} q v_{sat} \frac{k}{d}}{k q v_{sat}} = \frac{75(v_{sat} dt) G q v_{sat} \frac{k}{d}}{k q v_{sat}} \propto \frac{G}{d} dt$$

!!!

➔ Go thin!!



(Real life is a bit more complicated, but the conclusions are the same)

Full simulation

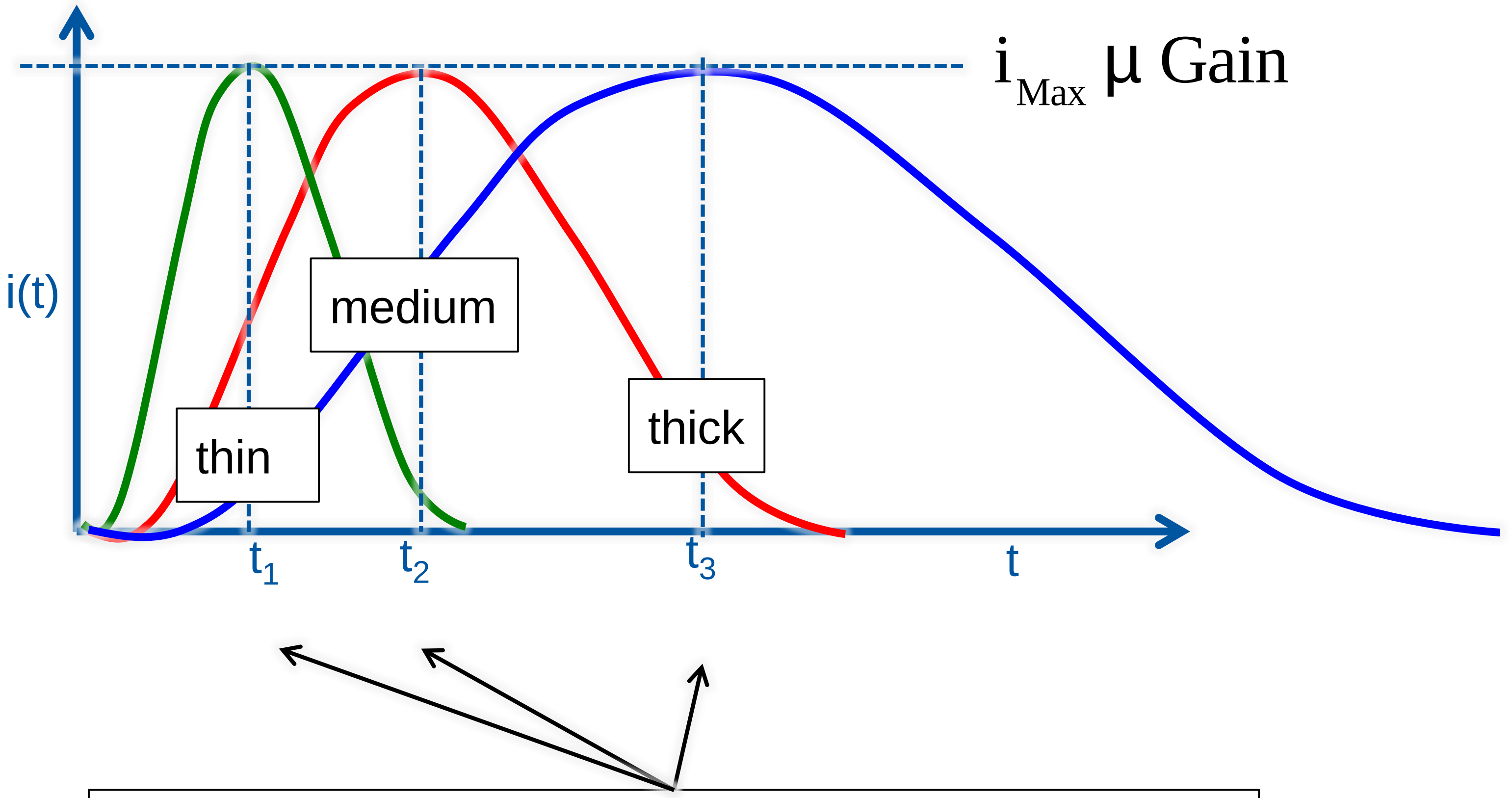
(assuming 2 pF detector capacitance)

300 micron:
~ 2-3 improvement with gain = 20

Significant improvements in time resolution require thin detectors

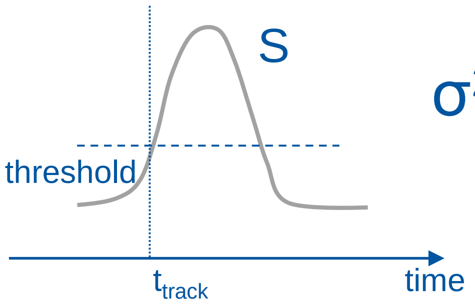
Gain and Signal current

$$\frac{dV}{dt} \mu \frac{G}{d}$$



The rise time depends only on the sensor thickness ~ 1/d

Time resolution



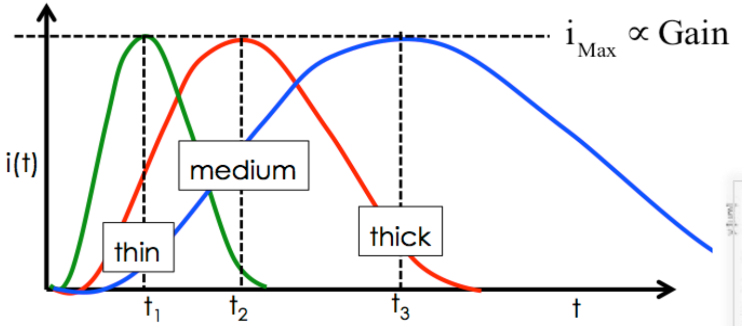
$$\sigma^2_t = \sigma^2_{Jitter} + \sigma^2_{Time\ Walk} + \sigma^2_{Landau\ Noise} + \sigma^2_{Distortion} + \sigma^2_{TDC}$$

Negligible
Optimize FE electronics

Negligible
Optimize RO electronics

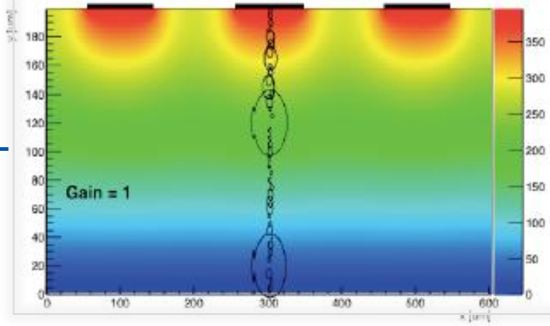
$\sigma_{Jitter} \approx N/(dV/dt) \approx t_{rise}/(S/N)$

➔needs **Gain** to increase S/N
➔needs **thin detector** to decrease t_{rise}



NB: signal amplitude DOES NOT depend on detector thickness

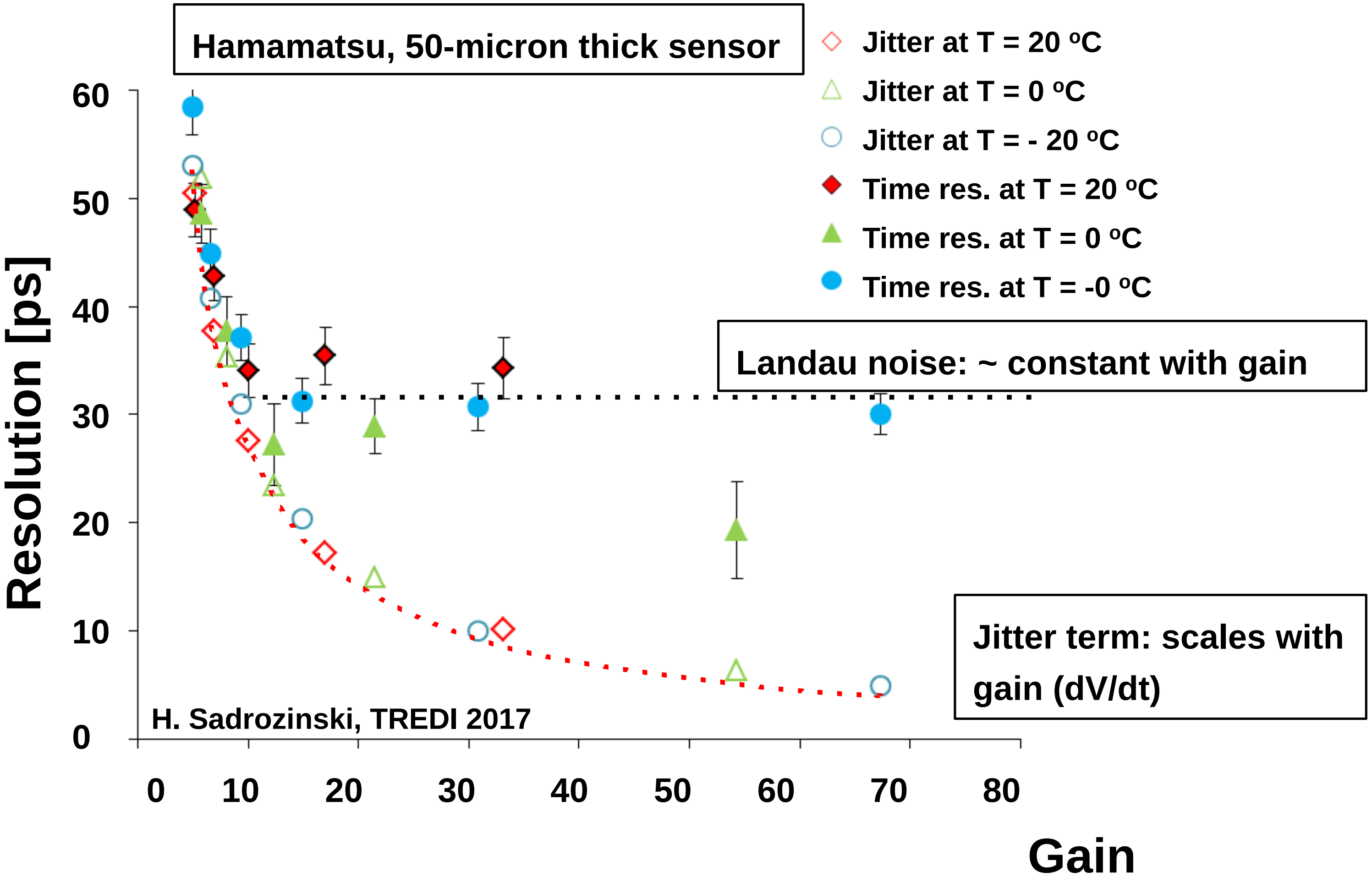
$I_{Ramo} \approx q\, v_{drift}\, E_w$
Requires **uniform v_{drift} and E_w**
⬇
parallel plate geometry
strip implant ~ pitch



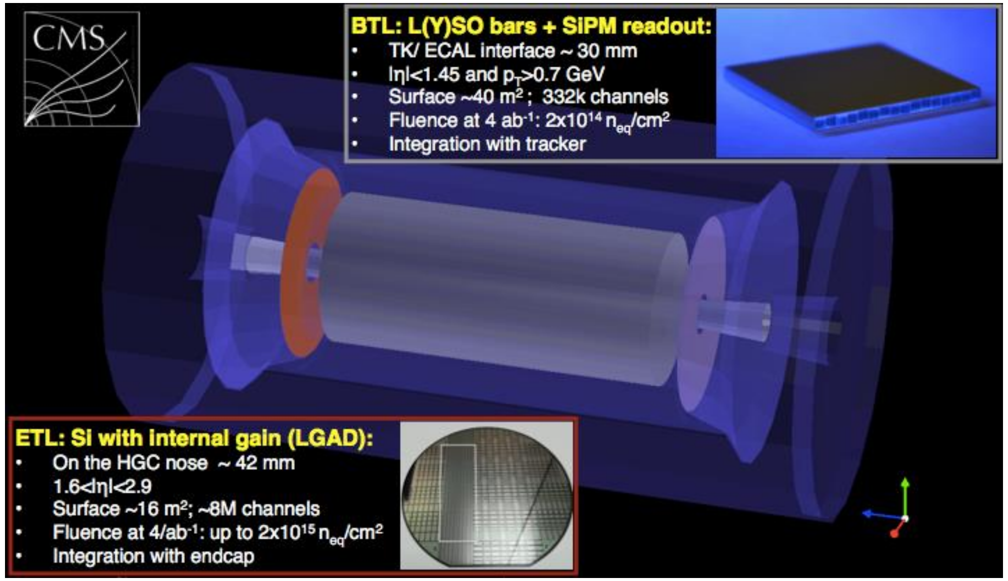
Decreases with detector thickness
Intrinsic Limit $\sigma_{Landau\ Noise} \approx 25ps$

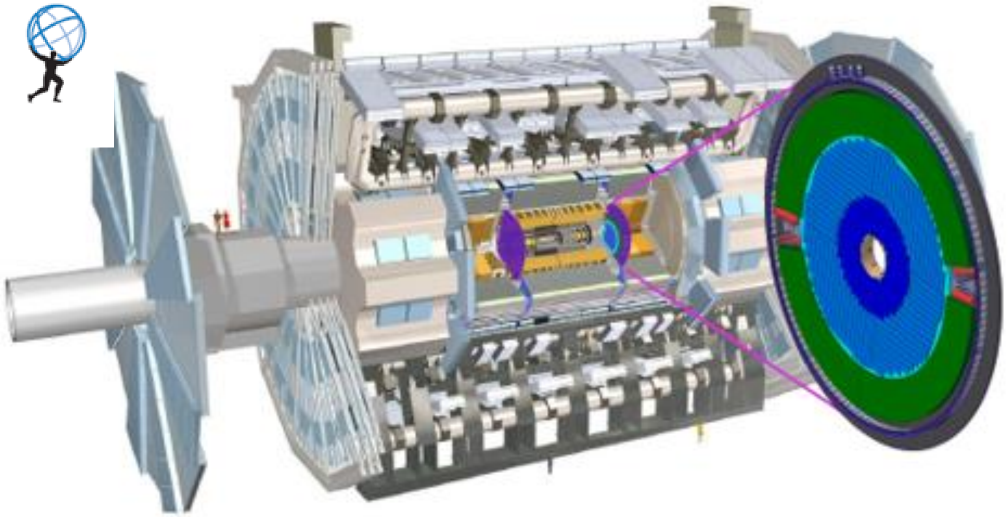
UFSD time resolution

UFSD from Hamamatsu: 30 ps time resolution,

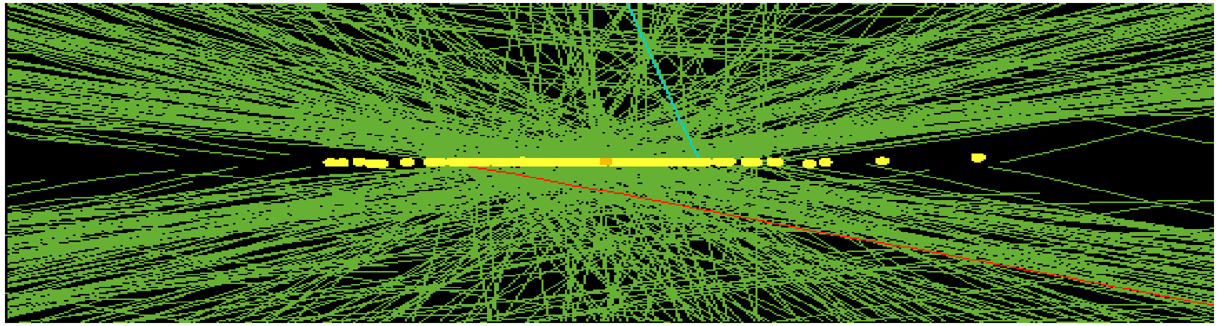


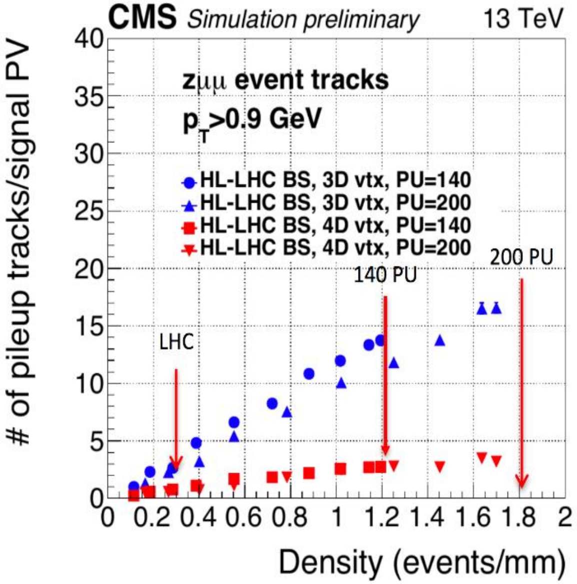
UFSD technology for CMS and ATLAS Endcap Timing Layers





At HL-LHC precise timing detectors will be used for Particle Identification and for pile-up suppression





A. Apresyan | Americas Workshop on Linear Colliders 2017

Add 30ps timing information

~x5 pileup (@ PU=200) reduction in terms of associated tracks

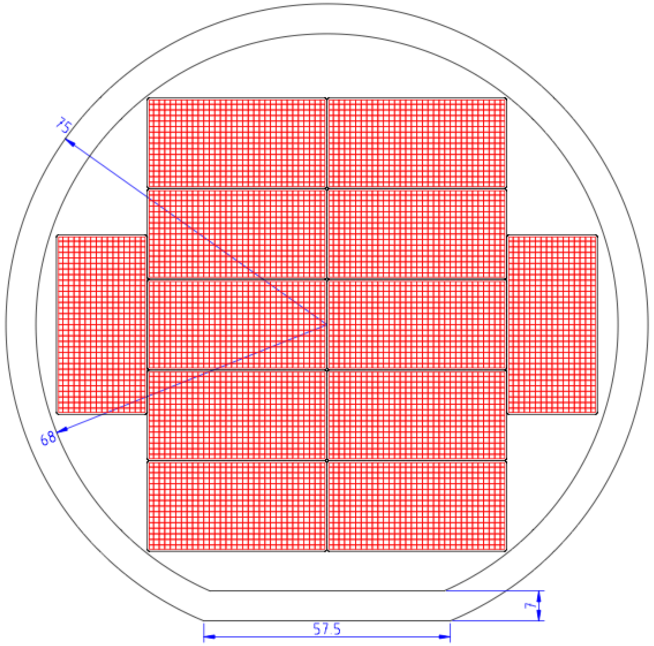
M.Costa – CEPC Workshop IHEP – 19 Nov 2019

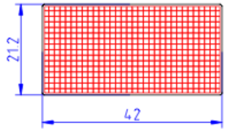
UFSDs for CMS ETL

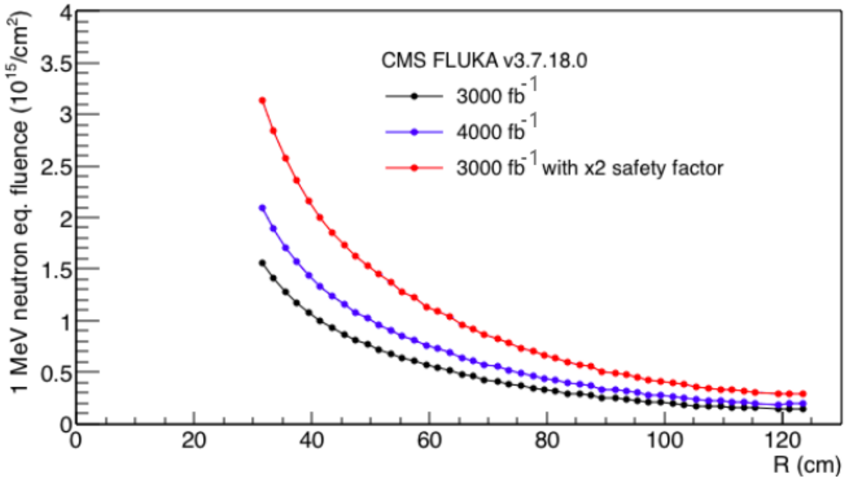
Using UFSDs for a “CMS size” detector poses many challenging

Sensor specifications:

- Intrinsic Gain: 10-20
- Pad size: 1.3 x 1.3 mm^2
- High fill factor (>85% per layer)
- 2-disk x-y layout
- Number of sensors: ~18000 (~ 16 m^2, ~2k 6-inch wafers)
- Sensors of 2x4 cm^2
- Radiation hardness

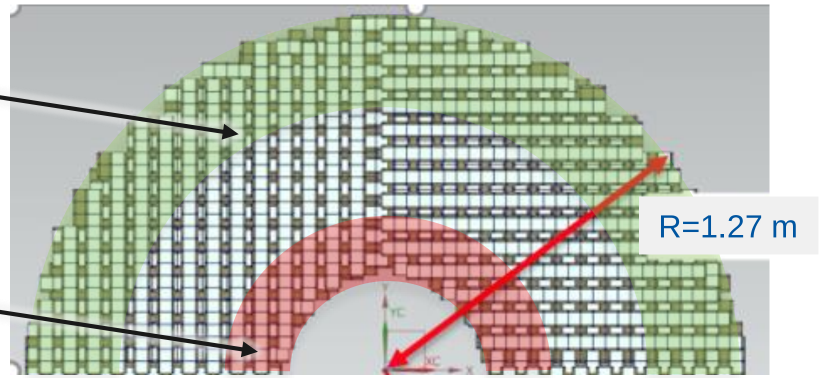






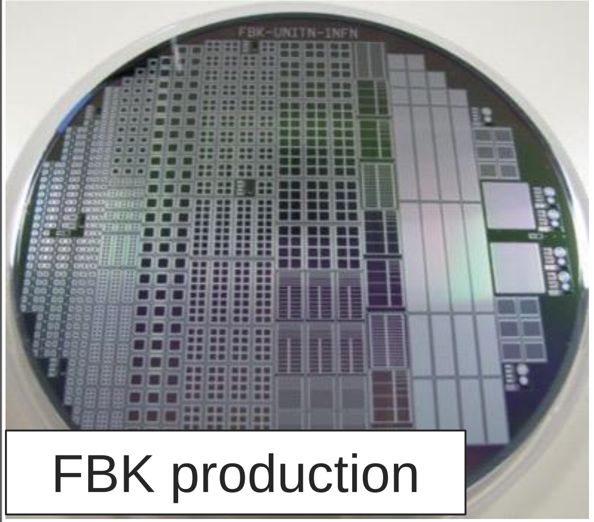
Less than 4×10^{14} n_{eq}/cm^2 for 50% of sensors

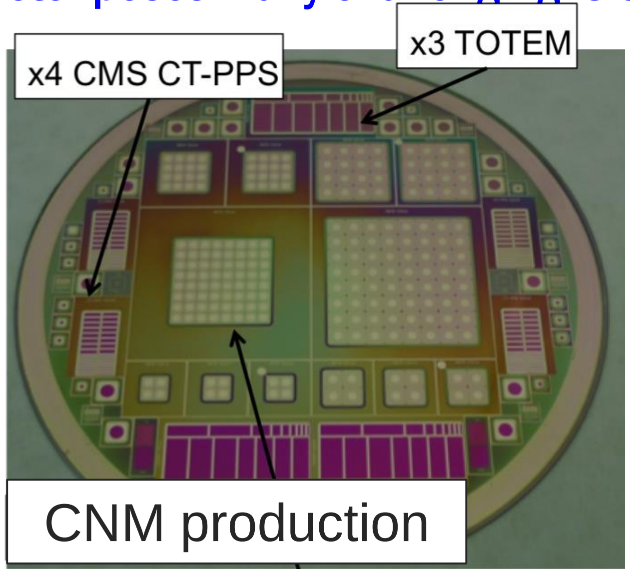
Up to 2×10^{15} n_{eq}/cm^2 for 15% of sensors

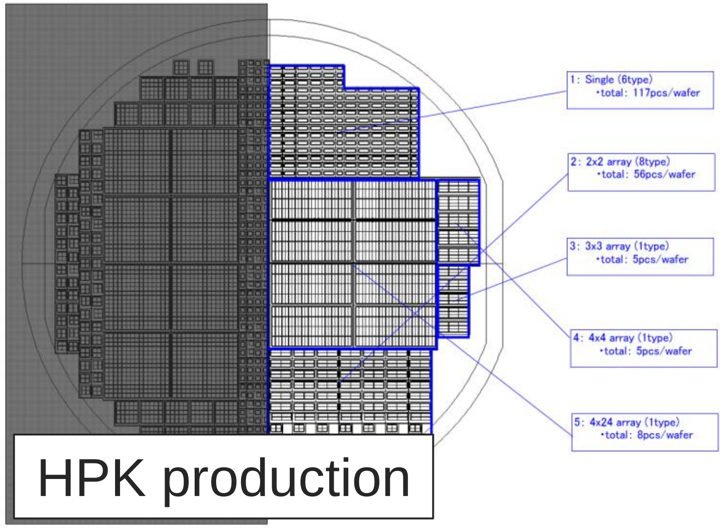


Foundries Producing LGADs for the CMS MTD

Using LGADs for a "CMS size" detector poses many challenging: 3 sensor producers considered so far







Producers have different approaches for radiation damage mitigation, but all vendors can fulfil the CMS requirements, **including a factor of 2 safety margin**

CMS1 delivered in Q3 2018

Next production: Q1 2020

CMS1 production is due to arrive in Q1 2020

Next production: Q1 2020

- **Q3 2021: Sensor vendor qualification and final geometry selection**
- **Q3 2022: Sensor vendor selection and pre-production start**

ON SCHEDULE

Up coming vendors:

Brookhaven National Lab, USA

NDL China → see Zhijun talk

Micron, England

UFSD time resolution summary

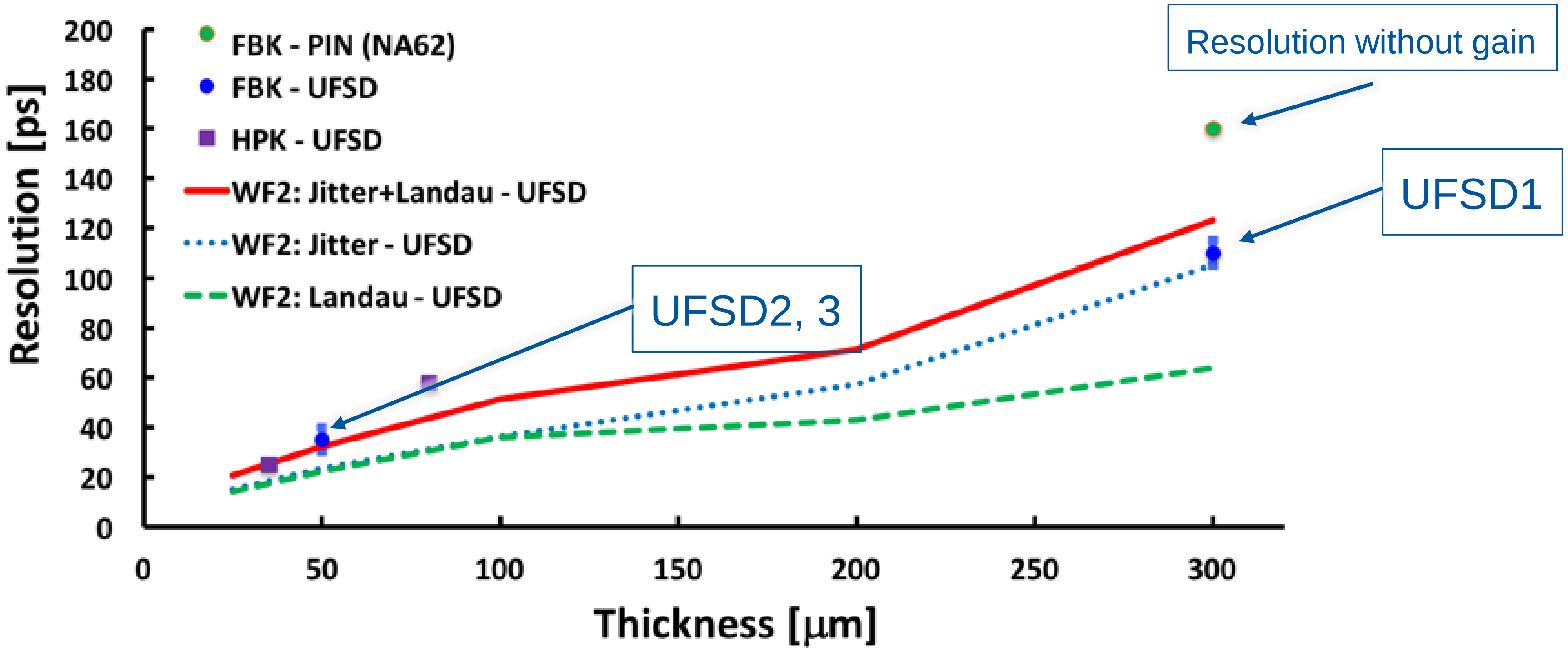
The UFSD advances via a series of productions.

For each thickness, the goal is to obtain the intrinsic time resolution

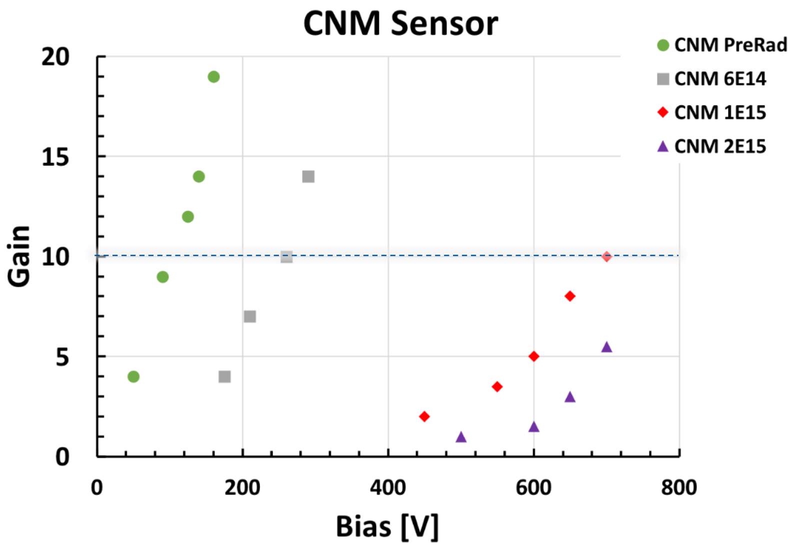
Achieved:

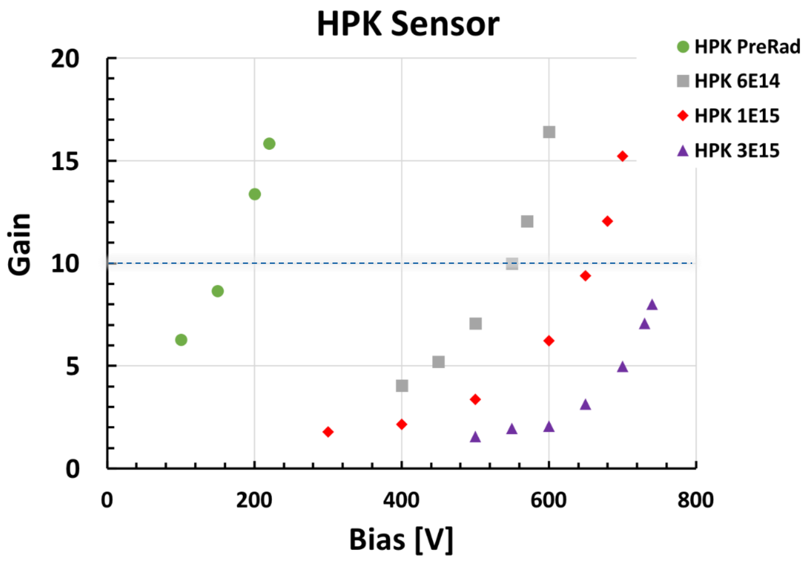
- **20 ps for 35 micron**
- **30 ps for 50 micron**

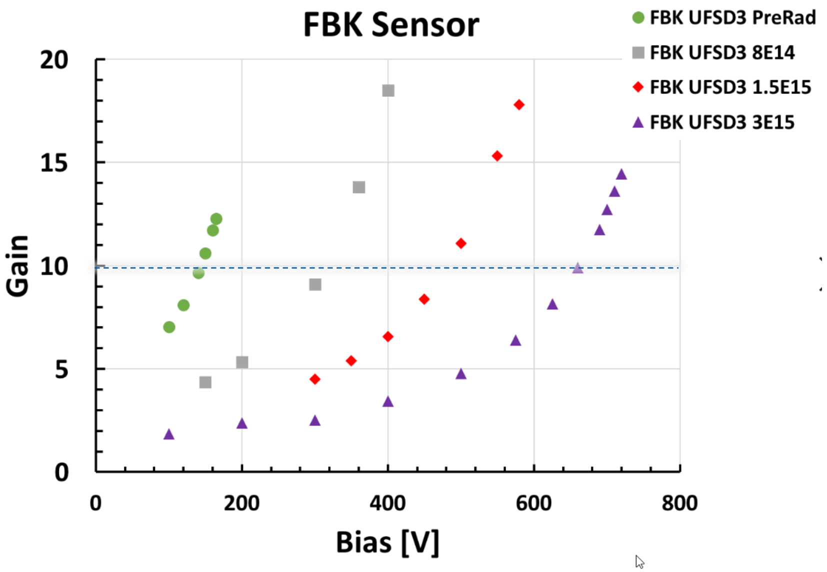
Comparison WF2 Simulation - Data
Band bars show variation with temperature (T = -20C - 20C), and gain (G = 20 -30)



Rad-Hard: vendors performances…so far





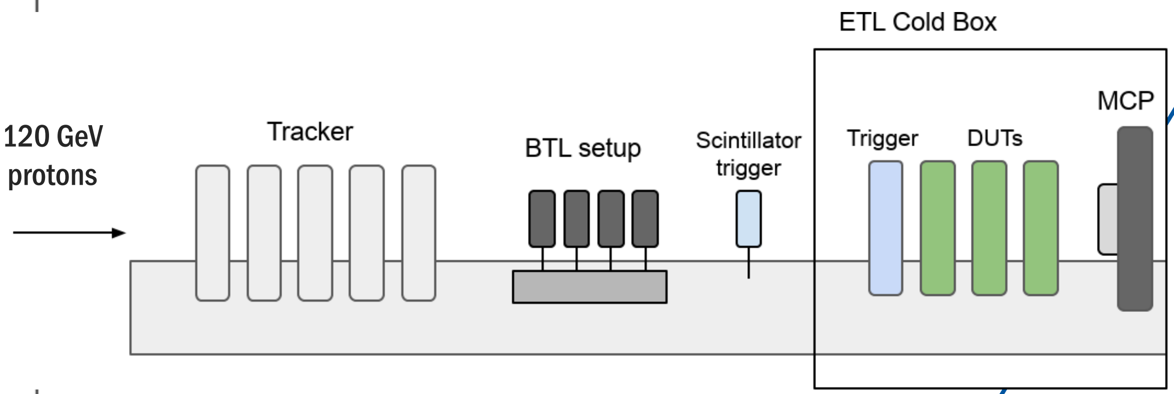


- **All vendors successful in delivering G = 10 till the end of HL-LHC (>10^{15} n_{eq}/cm^2)**
- CNM HPK similar behavior, while
- FBK, can reach G = 10 at lower Bias

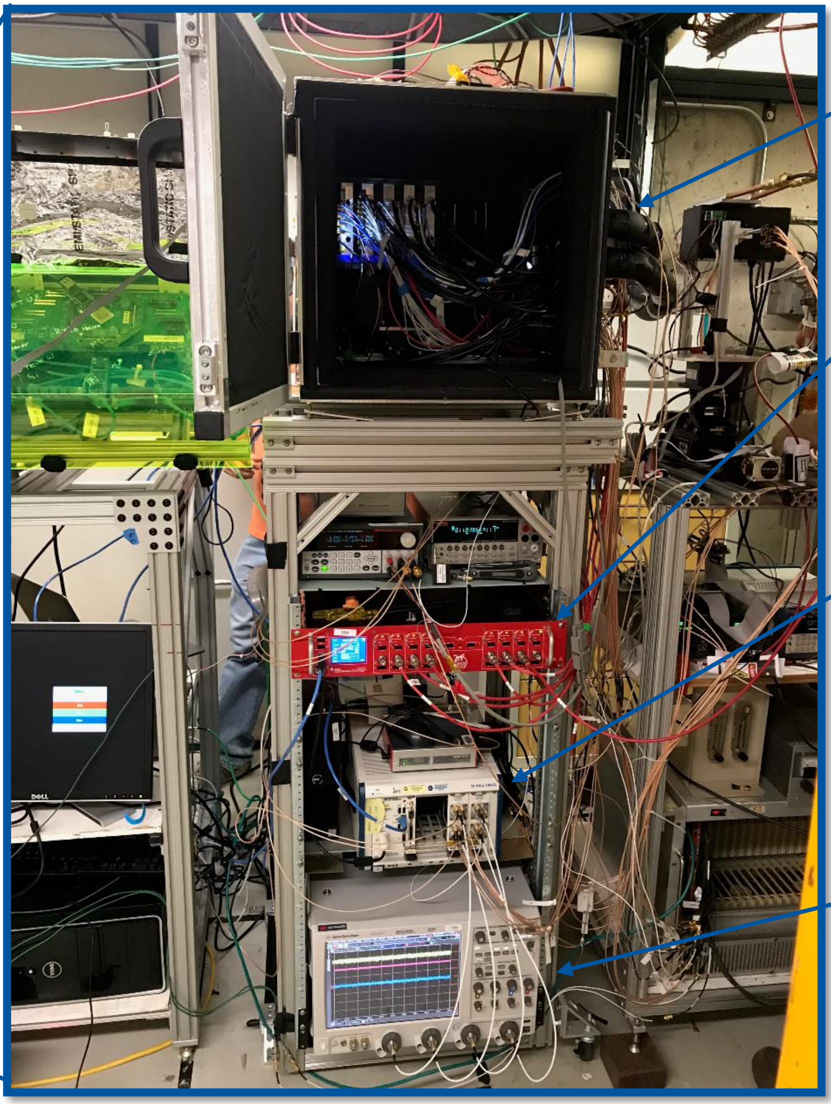
Refs:
https://arxiv.org/abs/1804.05449v2,
https://arxiv.org/abs/1707.04961,
https://doi.org/10.1016/j.nima.2018.08.040

FNAL Test Beam

LGADs were tested at FNAL using an MCP-PMT as time reference and a silicon tracker to measure efficiency and uniformity



Permanent mechanical structure: ETL cold box can slide in and out of beamline as needed



Cold box (5 boards)

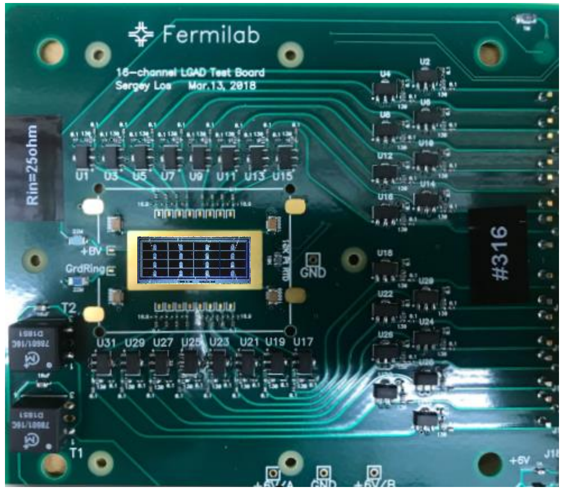
High Voltage

High BW multiplexer

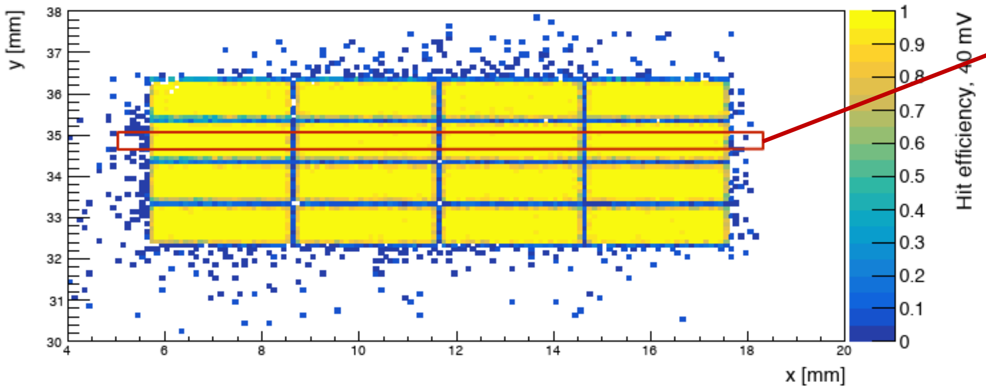
40 Gsa/s
100k events per spill
(possibility of using Sampic with 32/64 ch)

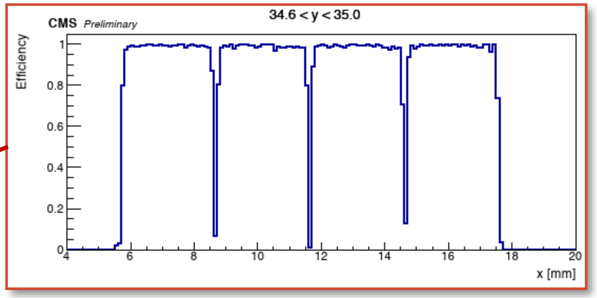
FNAL Test Beam: from single pad to arrays

Uniformity has been studied on 16 pads arrays using a 16ch readout board



Hit Efficiency



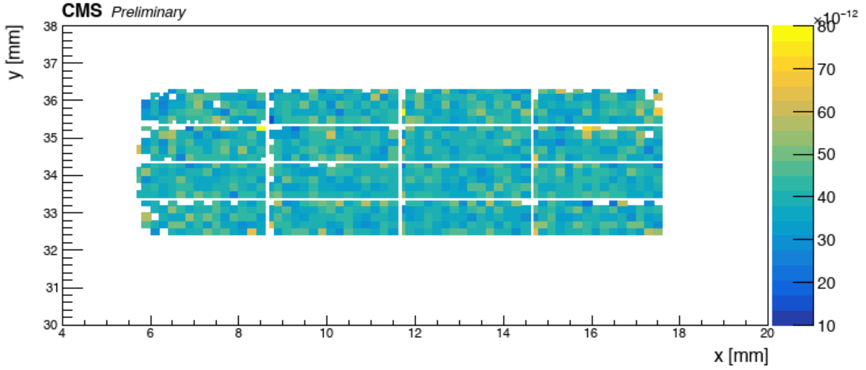


Efficiency >99% (except gaps)

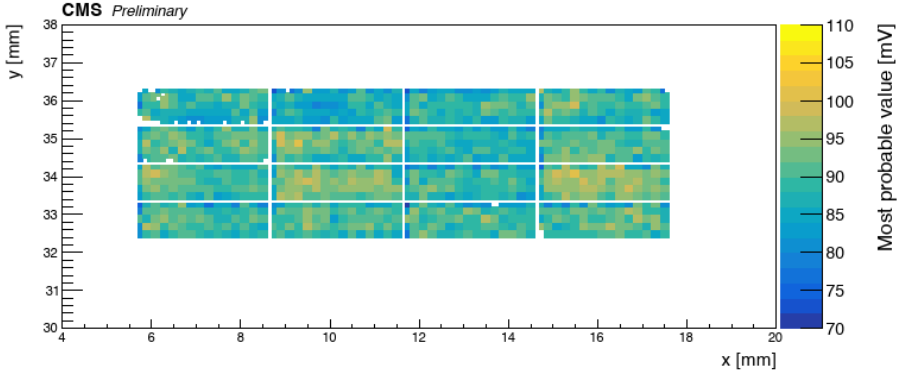
Interpad distance investigated:

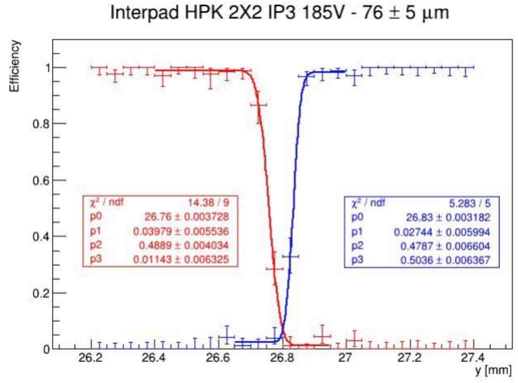
Fill Factor >85% per layer

Time Resolution



Most Probable Amplitude

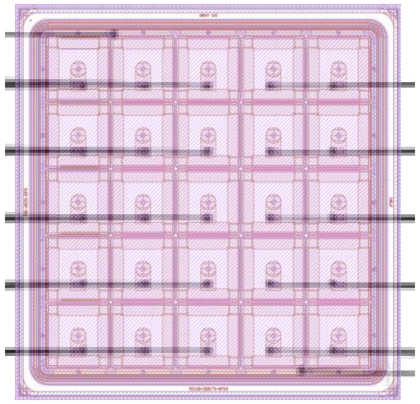




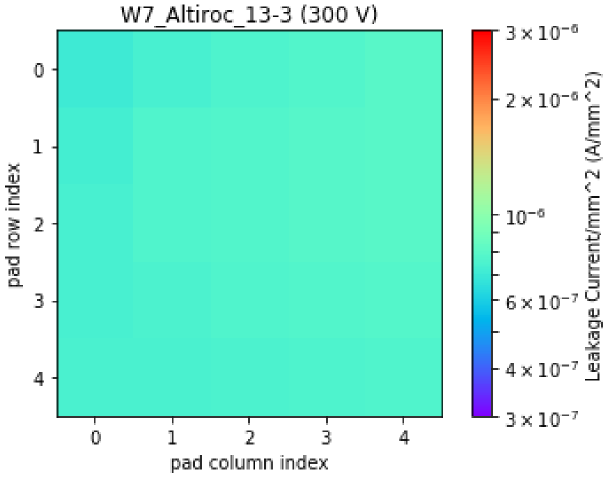
Uniformity checks: IV sensor characterization

It is impossible to test several m^2 of sensors using a particle beam: uniformity checks using automated systems

Using a probe card it is possible to measure automatically 25 pads



All pads have a similar current @300V



Very few channels have a leakage current away from the mode:

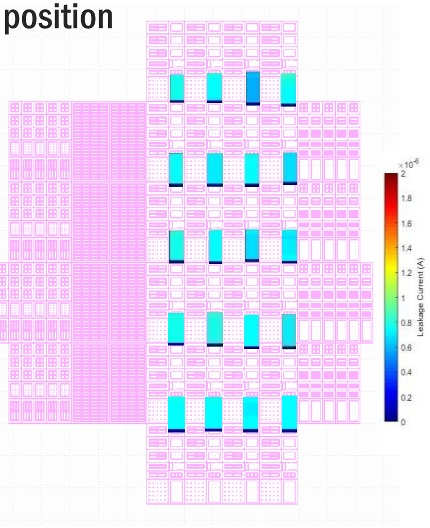
Table 3.4: Summary of the uniformity studies on the latest sensor productions.

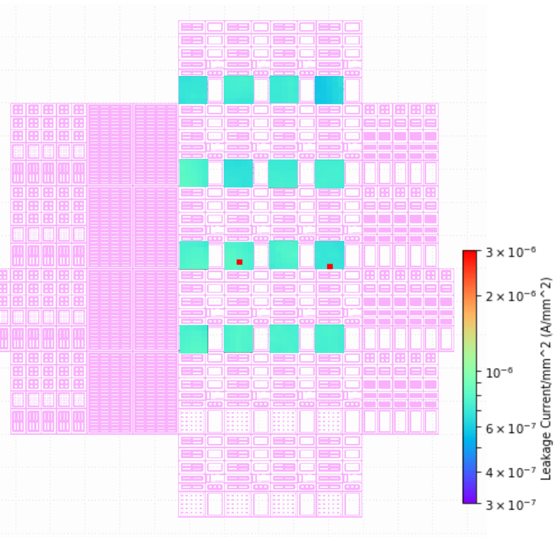
Foundries	Sensor type	# Sensors tested	# Warm pads	# Bad pads	Comments
FBK	4 × 24 pads	152	14 (0.1%)	0	bias = 100 V
FBK	5x5 pads	23	4 (0.7%)	0	bias = 300 V
HPK	4 × 24 pads	15	20 (1.3%)	0	bias = 250 V

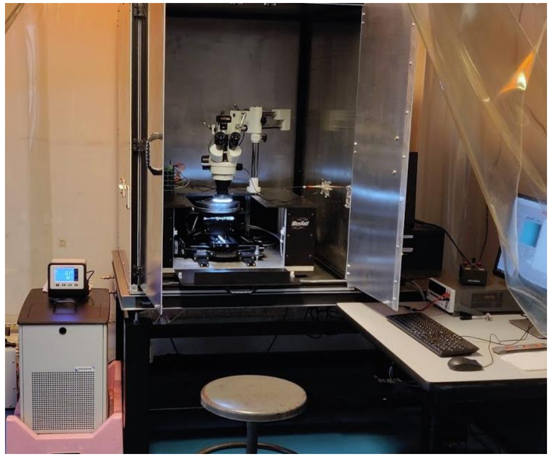
Leakage current > 10x the mode

Leakage current too high: sensor failure

Same test performed on sensors in different position on the wafer





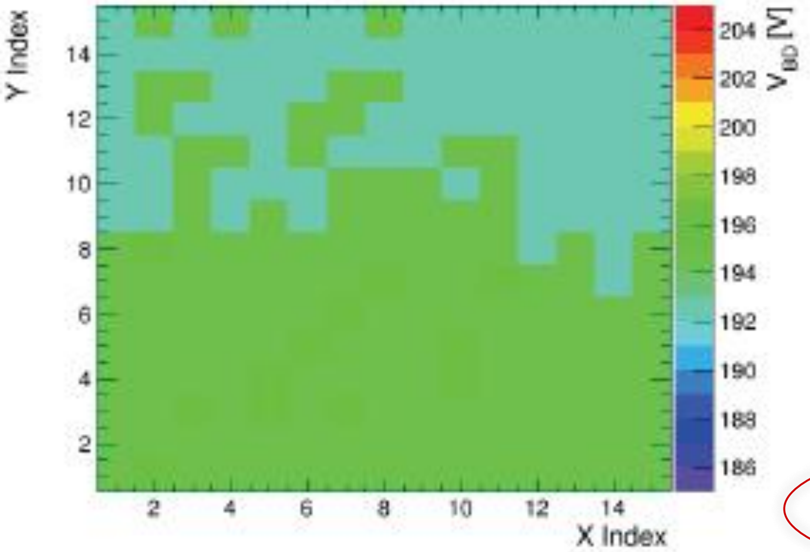


Fully automated **visual checks** and **IV characterization** of the 5-10% wafer under development

Arrays: 15 x 15 pads

- **Studies of 15 x 15 LGAD arrays on-going (half-size of final sensor)**
  - *Full size for HGTD: 30 x 15*
  - *2 x 4 cm²*

- Microscope photo of an HPK-ATLAS Type 3.1 15×15 array.



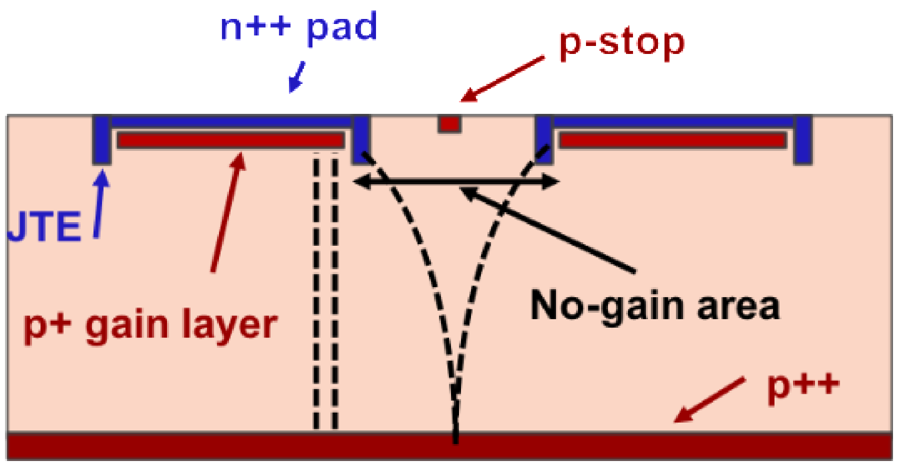
- **V_{BD} map of a 15 × 15 HPK type 3.1 array**
  - Measurement at room temperature
  - Neighbours and GR floating

- **Excellent uniformity observed**

- **Feasibility of large-size LGAD arrays demonstrated**

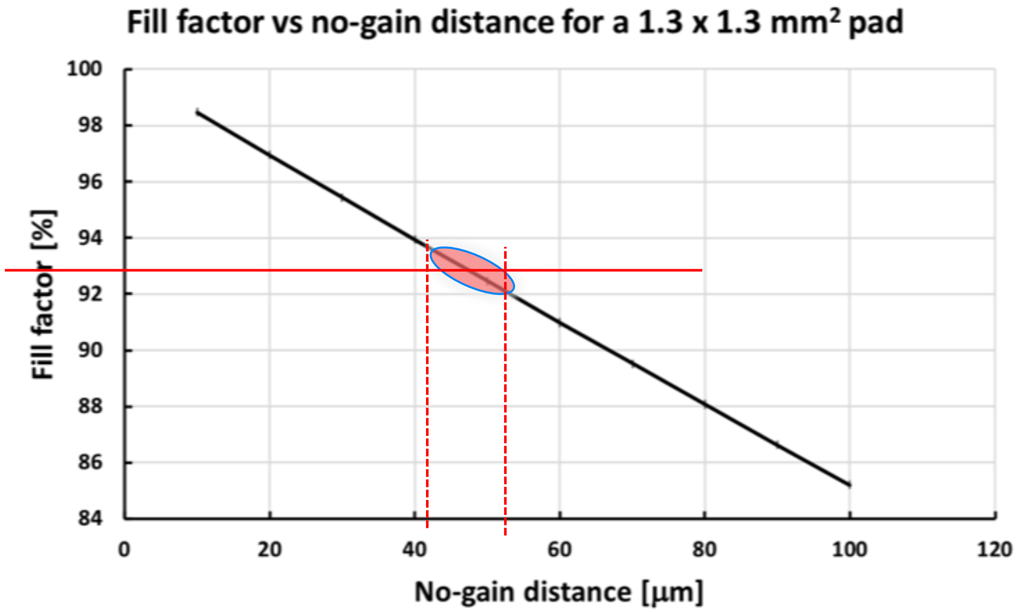
Status of interpad no-gain area

Foundries	No-gain distance [μm]	Comments
CNM	100	The latest production with smaller distances has very high leakage current and cannot be used. A new production is expected in August 2019
FBK	40, 70	In the latest production much smaller distances were attempted but the sensors go into early breakdown. A dedicated new production is expected in April 2019.
HPK	75, 90, 135	Even the shortest separation works well, most likely HPK can obtain even smaller distances.



Our goal is to have a fill factor of 85% per layer,

- 5% comes from the sensors placement
- 2-3 % dead area comes from the butting of sensors in the module
- 7-8% comes from the no-gain area

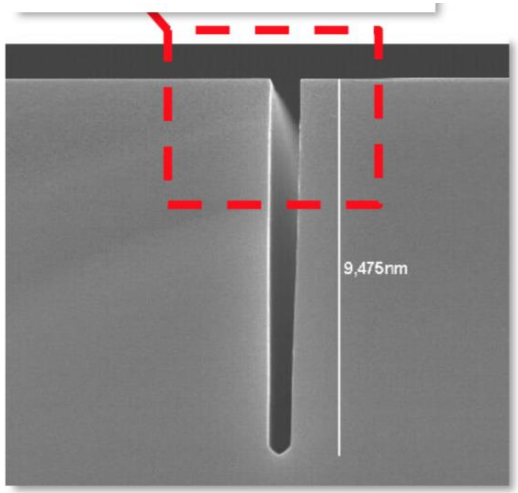


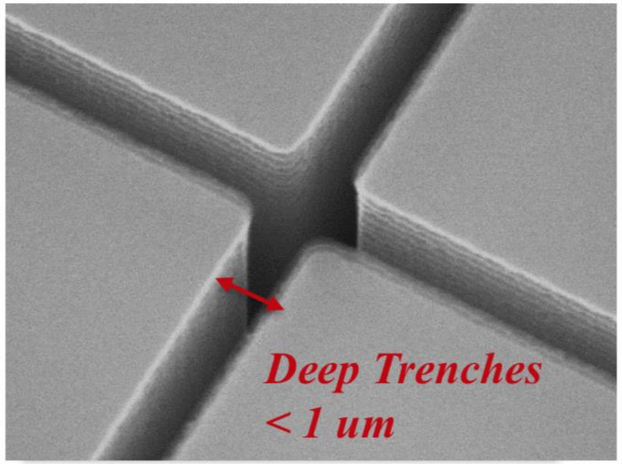
New: TI-LGAD replace p-stops with trenches?

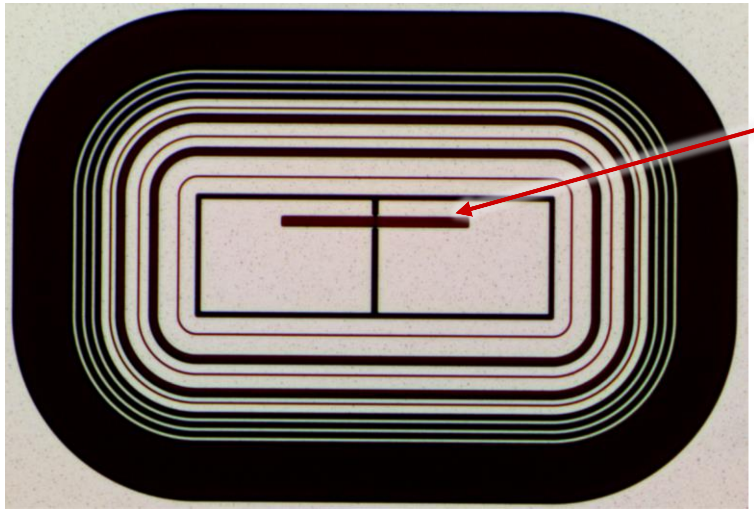
Trench isolation technology

- Typical trench width < 1 um
- Max Aspect ratio: 1:20
- Trench filling with: SiO_2, Si_3N_4, PolySi

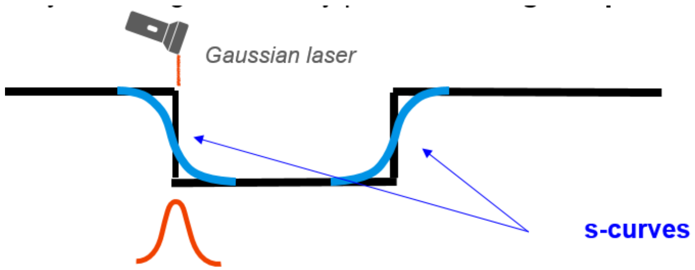
CMM
CENTRE FOR MATERIALS AND MICROSYSTEMS





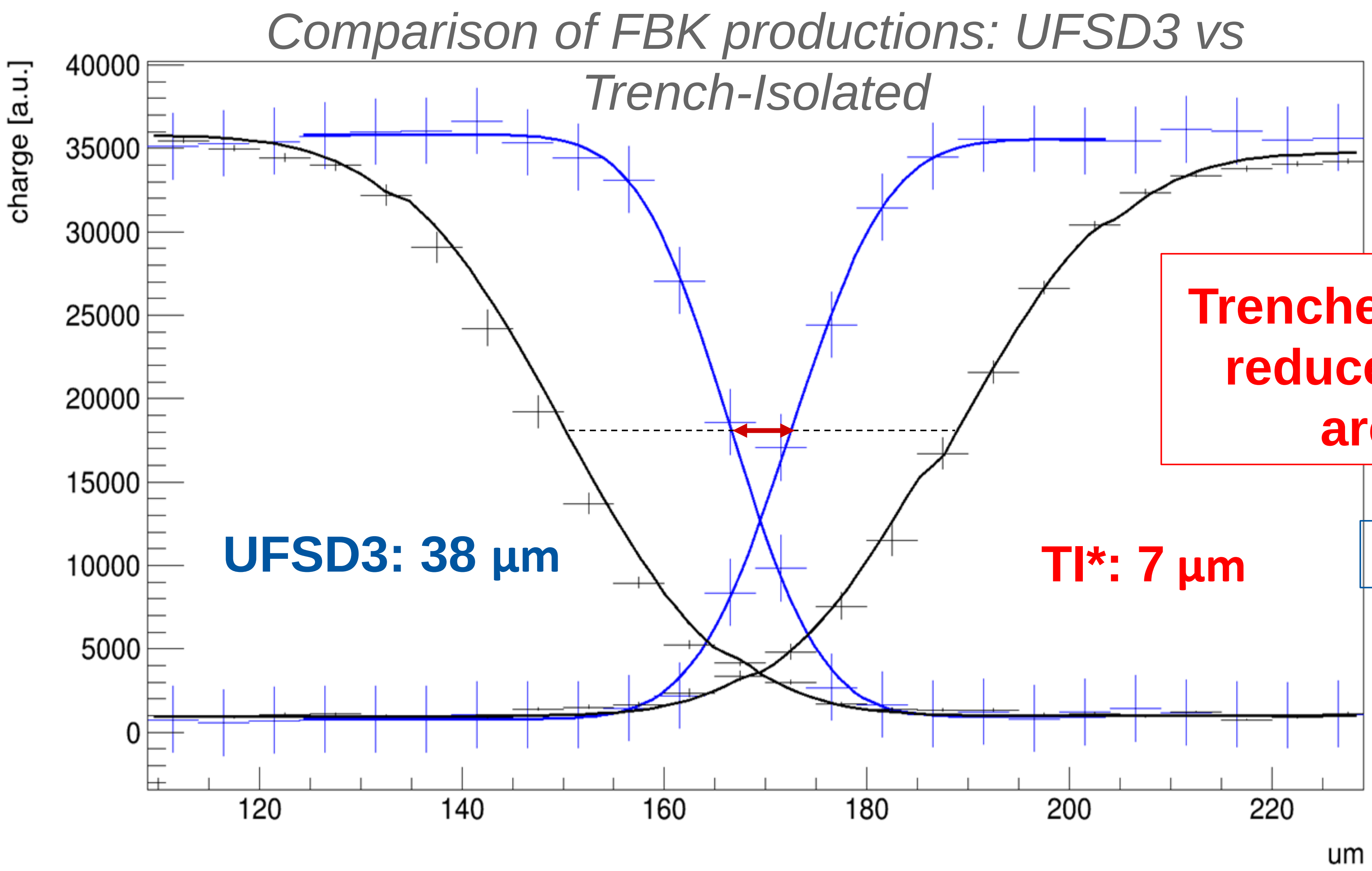


- **2x1 TI-LGAD** (by FBK) with optical window for laser testing **(TCT technique)**
- Shoot with laser on one pad to **prove it is isolated from the neighbouring one**
- Both pads read-out, connected to an oscilloscope



-1030 nm laser
- spot is 10-15 μm with a gaussian shape

Trench Isolated vs standard LGAD



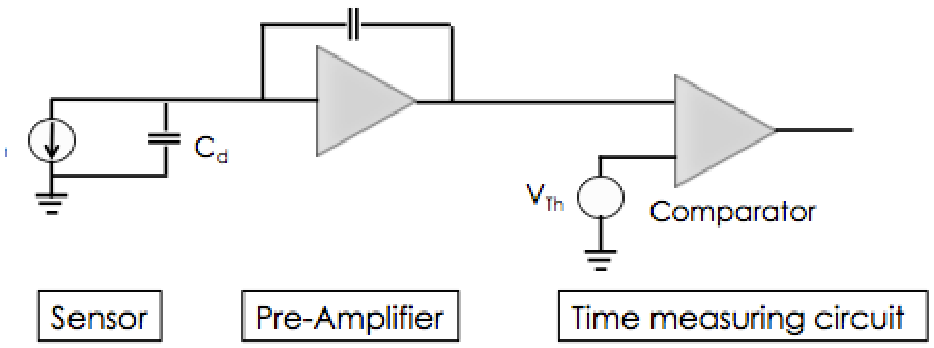
Trenches significantly reduce the inactive area width!

Fill factor > 95% !

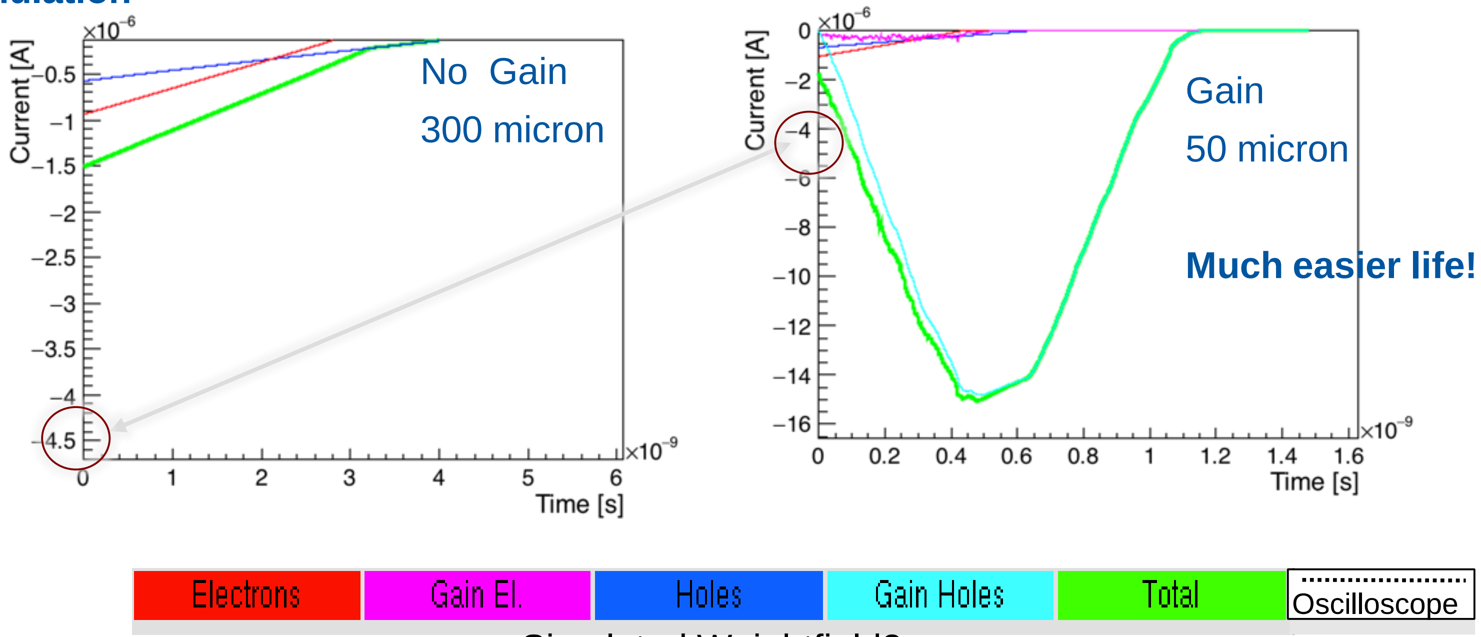
Electronics

To fully exploit UFSDs, dedicated electronics needs to be designed.

The signal from UFSDs is different from that of traditional sensors



WF2 simulation



Simulated Weightfield2

Pads with no gain

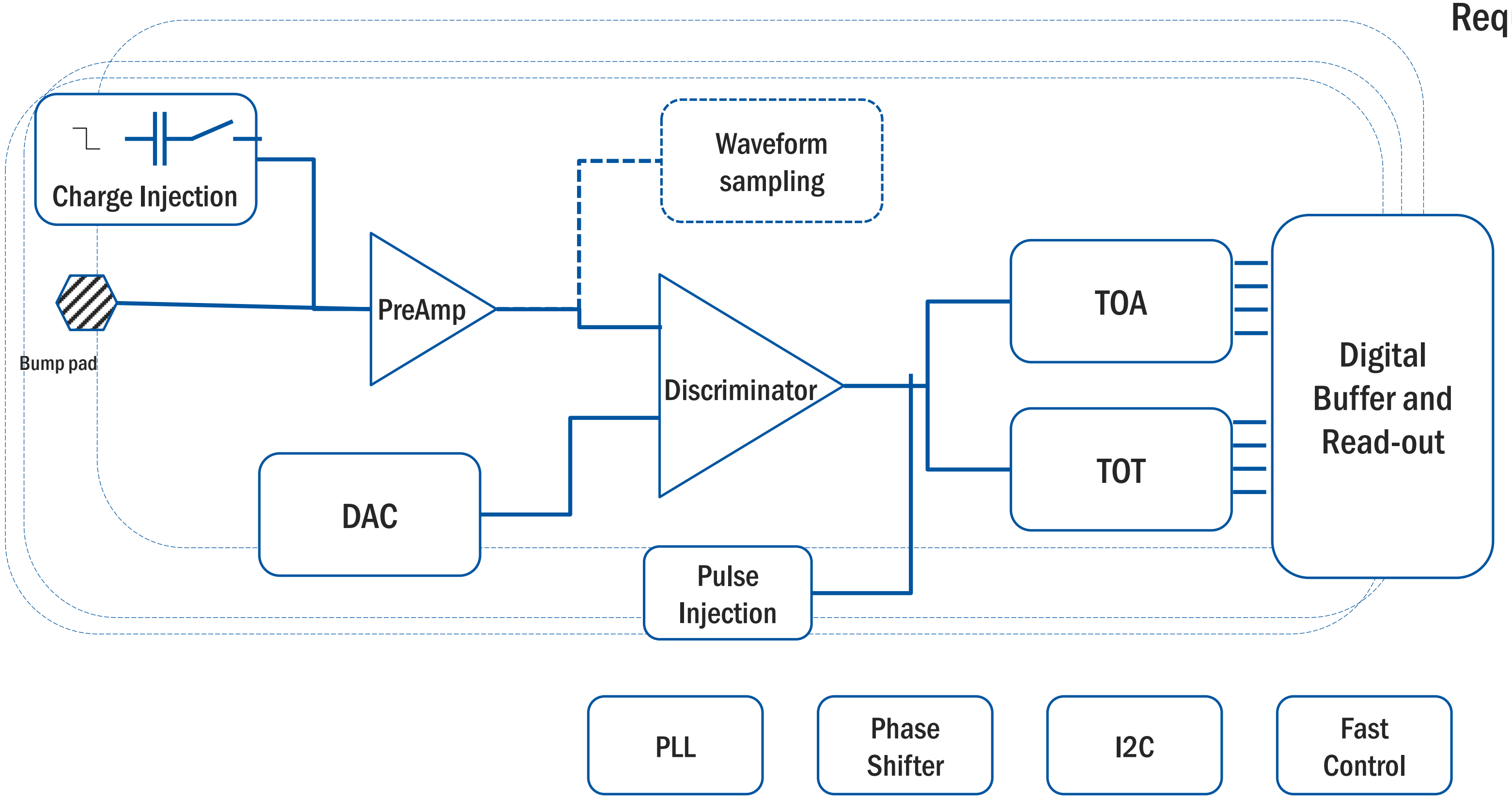
Charges generated uniquely by the incident particle

Pads with gain

Current due to gain holes creates a longer and higher signal

ETROC: CMS read-out ASIC for ETL

ETROC, currently under design at FNAL CMOS 65 nm technology, will be able to read out 16 m^2 of UFSDs, measuring the time of arrival with a precision better than 50 ps per hit (<30 ps per track)



Requirements:

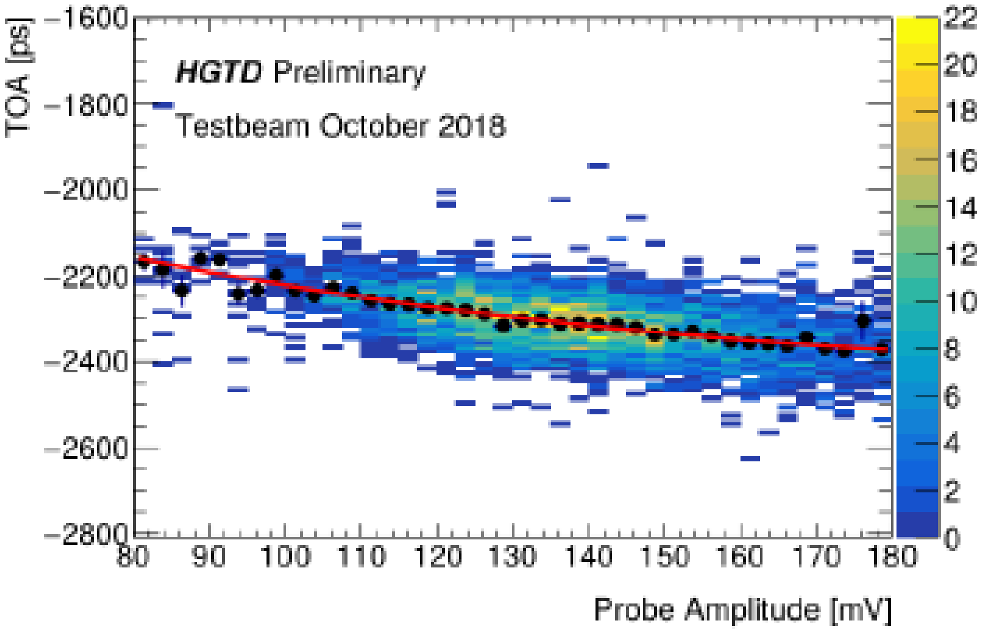
- < 50 ps per hit: ASIC contribution <40 ps
- Pad Size: 1.3x1.3 mm^2 , 50 micron thick
- Input capacitance: 3.4 pF
- MPV for MIP: ~6 fC for UFSD @ 10^{15} neq/cm^2
- Buffer latency :12.5 μs
- Trigger rate: Up to 1 MHz
- Time Of Arrival: ~ 5 ns windows
- Time Over Threshold: ~ 10 ns windows
- Power consumption: <4 mW/ch (80 kW total)

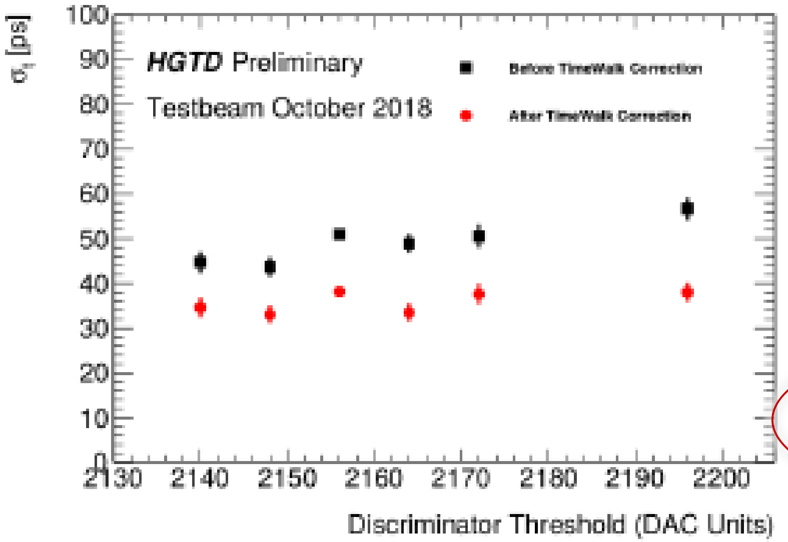
Post layout simulations being validated with lab tests of ETROC v0 (preamp+ discrim)

ALTIROC Studies

- **Testbeam results from ALTIROC0 bump-bonded to 2x2 array**

- **TOA variation** as a function of the amplitude of preamplifier output
  - Correction for time walk with polynomial fit

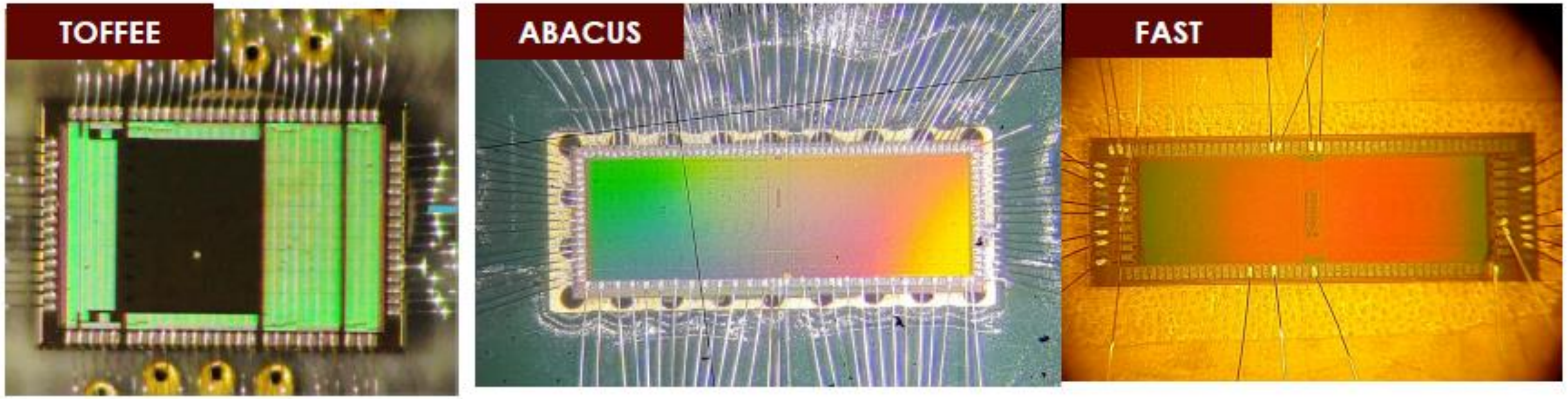




- **Time resolution** as a function of the threshold

- **Can achieve 35 ps with timewalk correction**
  - *Includes both sensor (~ 25 ps) and jitter*
  - **Jitter deduced to be ~ 25 ps**

ASICs developed for applications with UFSD



Developed @ INFN-Torino

FAST

TIME

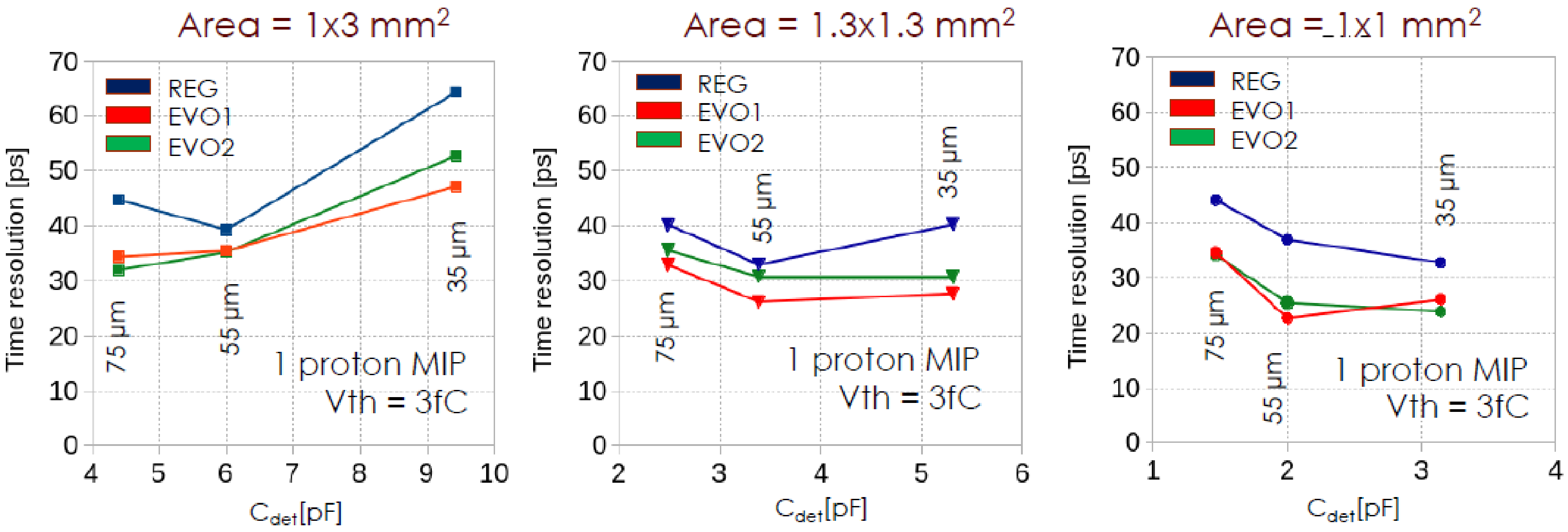
ASIC	Application	#ch	mm²	mW/ch	technology	FoM	Production
TOFFEE	Timing	8	3.6x2.5	20	110nm	45 ps (8 fC MIP)	2016
ABACUS	Single ion counting	24	5x2	15	110nm	3-130 fC Qin @ 100 MHz	2018
FAST	Timing and counting	20	5x1.7	3	110nm	25 ps Jitter (8 fC MIP)	July 2019

- **FoM**: picosecond time resolution and single ion detection at high rates (e.g. particle therapy applications)
- **Main challenges**: low power budget (<1.5 mW/Ch) and large sensor capacitance (6pF)

FAST Time resolution vs sensor area and thickness

INFN

- Study done playing with three important parameters:
  - → **Sensor thickness:** 35 µm, 55 µm, 75 µm → 3 values of C_{det}
  - → **Sensor geometry**: 1x1 mm², 1.3x1.3 mm² and 1x3 mm²
  - → **Front-end:** REGULAR, EVO1 and EVO2



Post layout simulation.
Exp results by Q1 2020

15th Topical Seminar on Innovative Particle and Radiation Detectors | Jonhatan Olave | Siena 17th October 2018 14

Electronic dominates balanced Sensor dominates

$$\sigma_t^2 = \sigma_{sensor}^2 + \sigma_{jitter}^2 + \sigma_{digit}^2 + \sigma_{clock}^2 + \sigma_{walk}^2$$

First production of 50-µm-thick Resistive AC-Coupled Silicon Detectors (RSD) at FBK

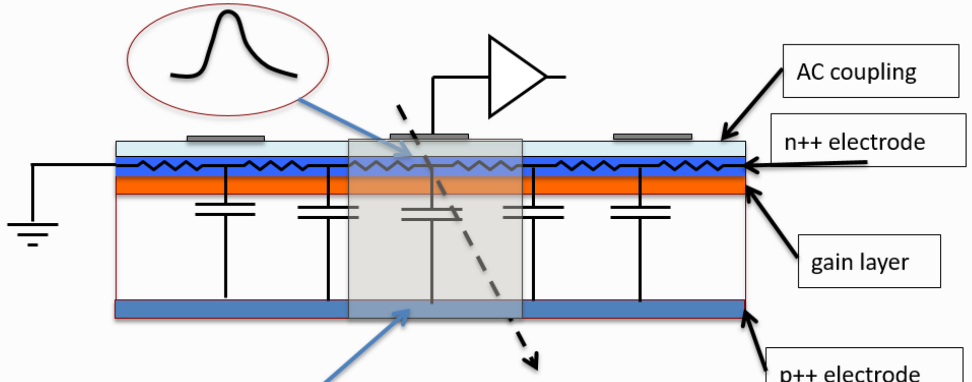
Marco Mandurrino * +

INFN Torino

* marco.mandurrino@to.infn.it
\+ on behalf of the **RSD project**

2019 IEEE Nuclear Science Symposium (NSS) – 29 October 2019 – Manchester (UK)

→ 100% fill factor
→ Segmentation is achieved via AC coupling



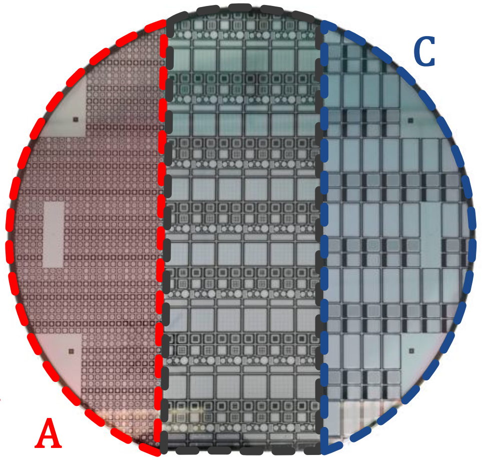
The AC read-out sees only a small part of the sensor:

3×3, **4×4** pads with **500×500** µm² **pitch**
5×5 pads prototype for **ATLAS/CMS**

75 µm **pitch** strip module for **PSI**

Square Matrix **Sensors:**

2×2, **3×3**, **5×5**, **8×8**, **10×10** pads
50×50 to **300×300** µm² **pitch**
different pad size
pin diodes



64×64 pixel with **50×50** µm² **pitch** sensor for **RD53A ROC**
180 µm **pitch strip** module for particle therapy

RSD1 testing campaigns

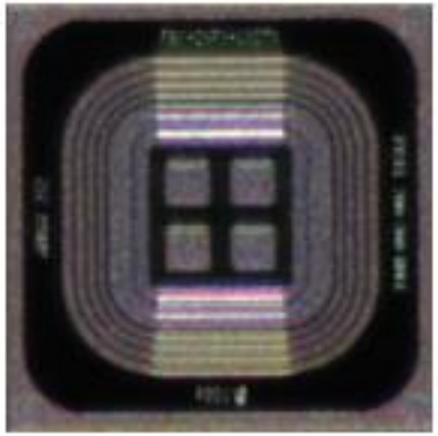
Time resolution: Sr 90 β-setup*

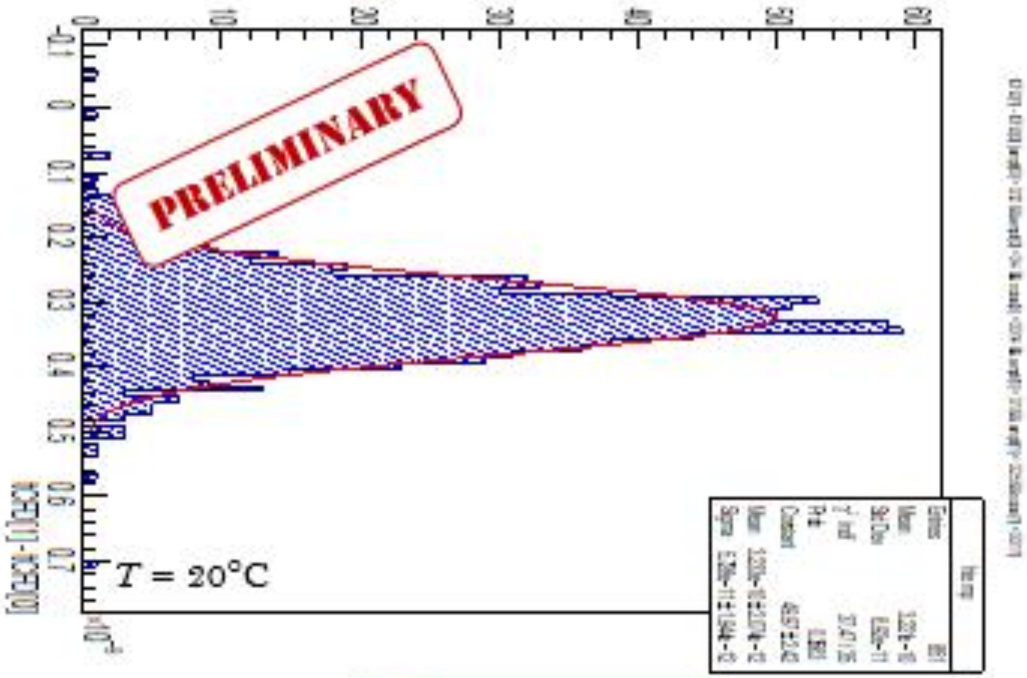
Tested sample:

- **2×2** matrix,
- **290/300** μm (pad size/pitch)
- **W10**

gain dose:	0.96
n^+ dose:	B
p-stop dose:	B
t_{diel}:	High
substrate:	Si-Si

- V_{bd} ~ **430 V**





σ_{RSD1} ~ 40 ps

*many thanks to the SSD-Lab @ CERN

Conclusions

- LGAD is a mature technology
- Ultra Fast Silicon Detector design optimized for HL- LHC is progressing well:
  - Common ATLAS and CMS R&D
  - <40 ps time resolution at > 10^{15} n_{eq}/cm^2 is achievable
  - Test of large arrays proved
  - Gain uniformity proved
  - Trenched Isolation LGAD reduce inter-pad region to less than 10 micron
  - Test of "very large" number of sensors under development
- CMOS 65nm chip designs are on going:
  - ATLAS ALTIROC0 bonded to LGAD sensors performing as expected
  - CMS ETIROC0 being tested (test beam planned in Q1 2020)
  - < 50 ps per hit achievable with 50 micron thin LGAD sensor

CMS and ATLAS Timing Layers will be a benchmark for LGAD's application in future experiments

Acknowledgment

We kindly acknowledge the following funding agencies, collaborations:

- ▻ Horizon 2020, grant UFSD669529
- ▻ Horizon 2020, grant INFRAIA
- ▻ Grant Agreement no. 654168 (AIDA-2020)
- ▻ INFN, Gruppo V
- ▻ Ministero degli Affari Esteri, Italy, MAE, “Progetti di Grande Rilevanza Scientifica”
- ▻ MIUR, Dipartimenti di Eccellenza (ex L. 232/2016, art. 1, cc. 314, 337)
- ▻ U.S. Department of Energy, grant DE-SC0010107
- ▻ RD50, CERN

Backup

ETROC details

Summary

Table 3.5: A summary of ETROC requirements.

Requirement	Value	Comments
Process	TSMC 65 nm MS RF LP 2.5 V with metal stack `1P9M_6X1Z1U_RDL` (CERN)	
Power supply	1.2 V	
Timing resolution	40 ps	Total timing resolution per hit including 30 ps contribution from sensor is 50 ps.
Pixel size	1.3×1.3 mm^2	
Pixel capacitance	3.4 pF	50 μm thickness
Pixel matrix size row x column	16×16	
Power consumption	below 1 W/chip	
Data storage capability	12.8 μs	Level-1 trigger latency
Trigger rate	Up to 1 MHz	
Operation temperature	-30 °C to $+20$ °C	
TID	100 Mrad	
SEU	TBD	system requirements

Power consumption

Table 3.7: A summary of ETROC power consumption for each circuit component. The preamplifier, discriminator, and TDC values are obtained from post-layout simulation with conservative assumptions about occupancy and operating temperature. The SRAM and global circuitry power consumptions are conservative extrapolations from similar circuits used in the ALTIROC.

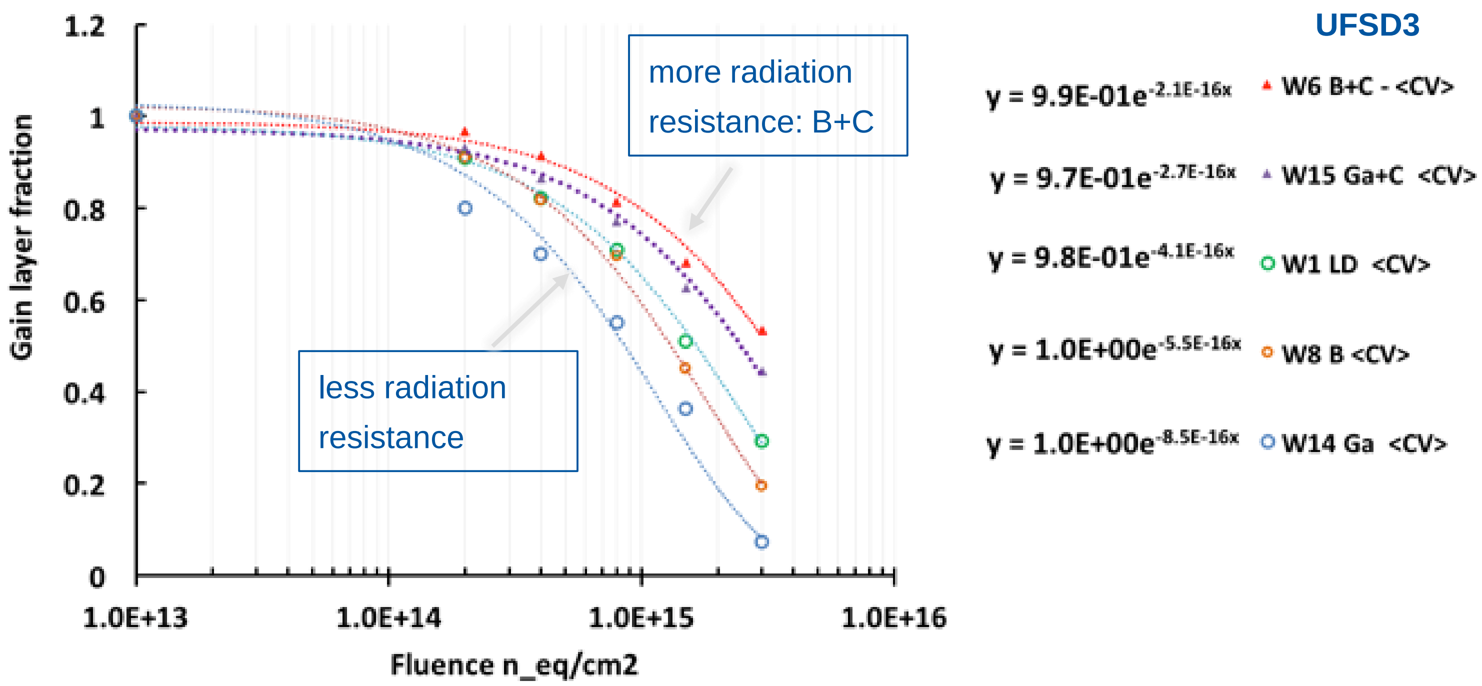
Circuit component	Power per channel [mW]	Power per ASIC [mW]
Preamplifier (low-setting)	0.67	171.5
Preamplifier (high-setting)	1.25	320
Discriminator	0.71	181.8
TDC	0.2	51.2
SRAM	0.35	89.6
Supporting circuitry	0.2	51.2
Global circuitry		200
Total (low-setting)	2.13	745
Total (high-setting)	2.71	894

Irradiation effects

Irradiation causes 3 main effects:

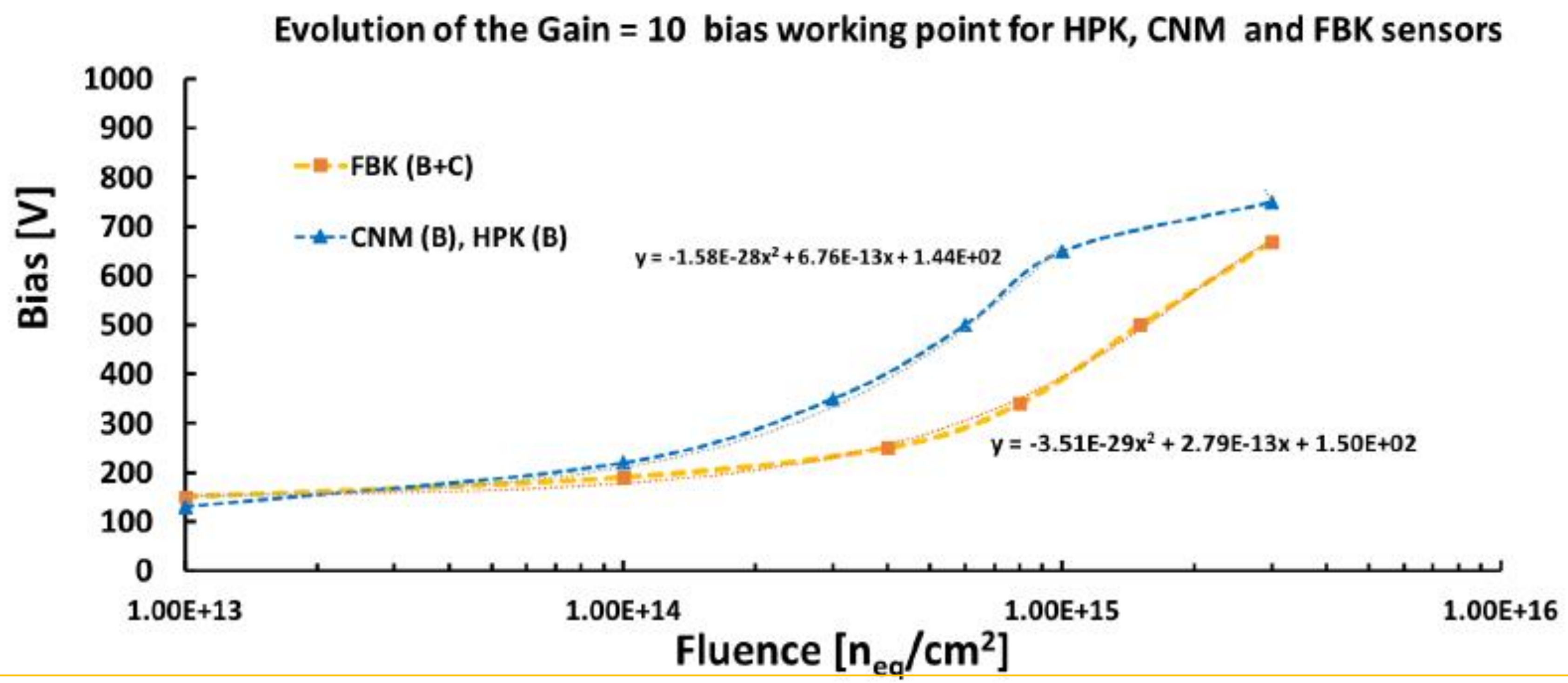
- Decrease of charge collection efficiency due to trapping
- **Doping creation/removal (the Gain fades)**
- Increased leakage current, shot noise

But…



Carbon addition works really well, increasing by a factor of 2-3 the radiation hardness

On the detector sensor biasing scheme

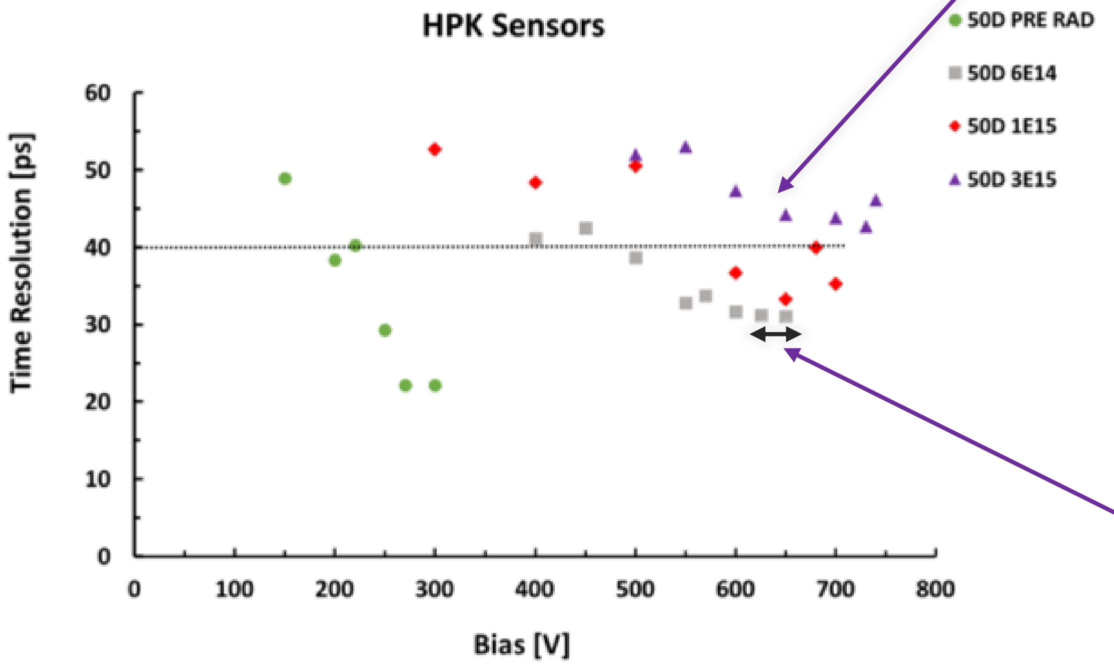


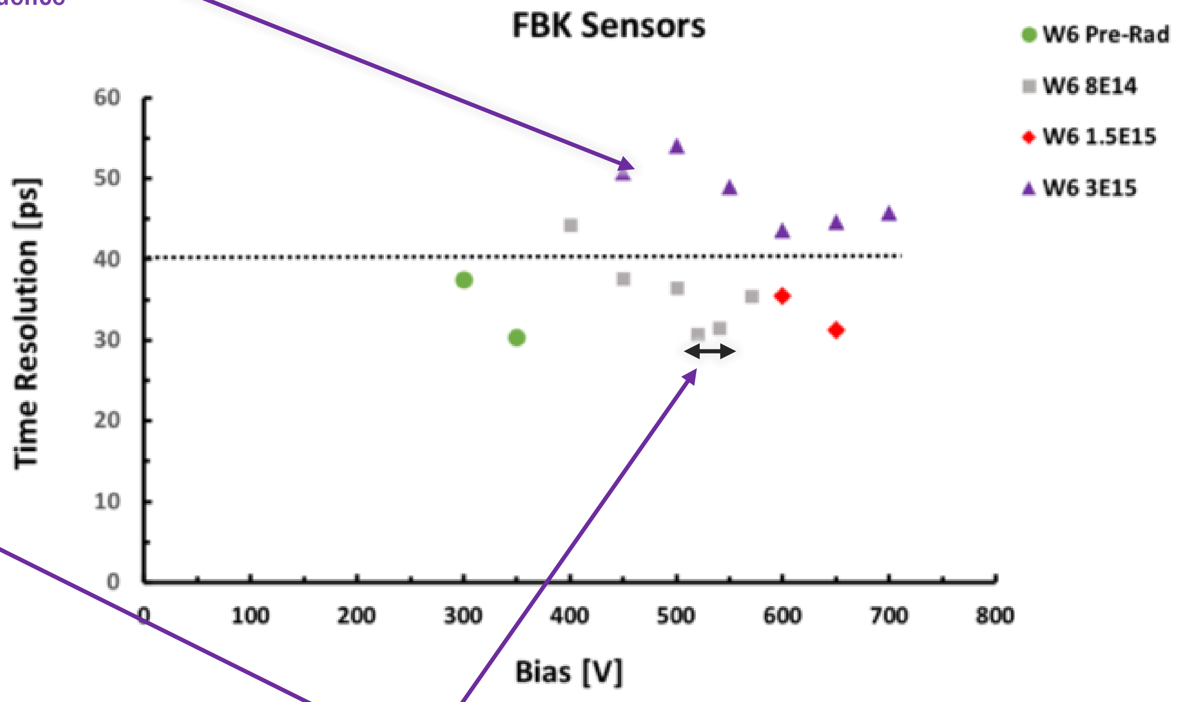
- Strong Bias increase needed to maintain G = 10 as a function of the irradiation level (FBK lower Bias than CNM,HPK)
- Detectors at different rapidity (radius) work at different Bias

Vendors performance … so far

Refs:
https://arxiv.org/abs/1804.05449v2,
https://arxiv.org/abs/1707.04961,
https://doi.org/10.1016/j.nima.2018.08.040

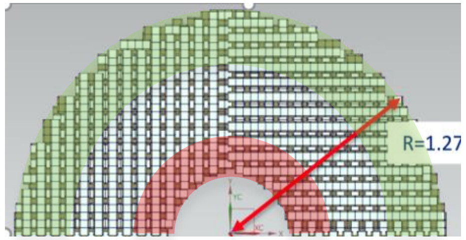
Time resolution





Both HPK and FBK sensors achieve **30-35 ps up to 1.5×10^{15} n_{eq}/cm^2**

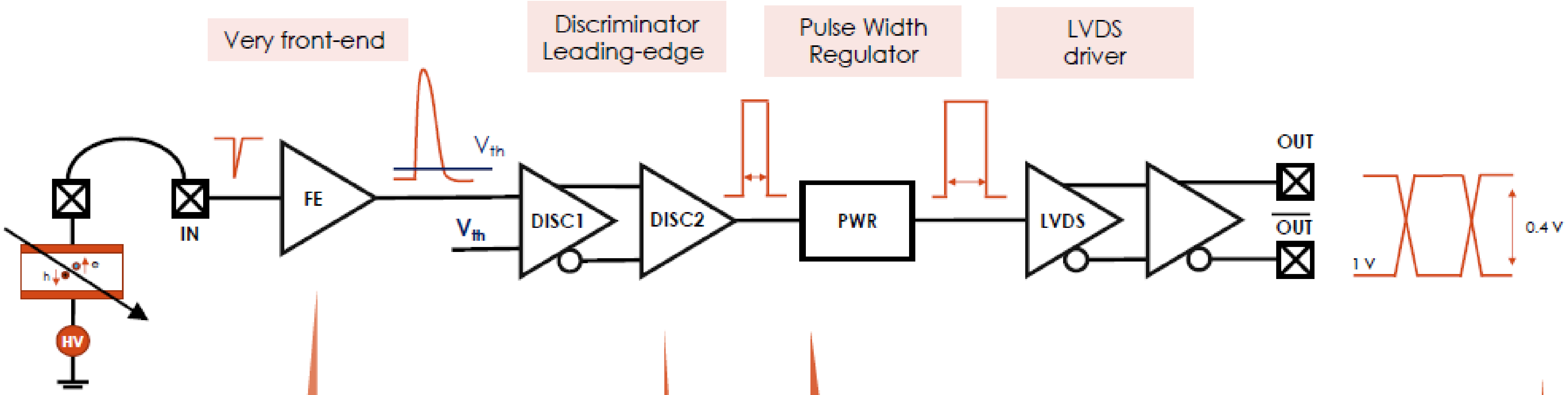
and 40-45 ps for 2x max fluence



Non uniform irradiation problem mitigated:

50V "undervolt" (we expect <30V) is not significantly affecting timing performance

FAST Front-end Amplifiers for Silicon detectors



The very front end

- **Three** architectures
- Power limited to **1.5 mW/CH**
- Designed for **1 proton MIP in 50 µm** thick UFSD sensor
- Sensor cap: **1 pF – 6 pF**

Discriminator

- Two stage leading-edge differential discriminator
- Power < **0.6 mW/CH**
- **time walk**
  → offline corrected

Pulse width regulator

- Pulse duration(MPV): **2-4 ns**
- This block can increase a regulated Δt to this duration to make it compatible with **commercial TDCs**

LVDS drive

- It allows compatibility with **commercial TDCs and FPGAs**