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A novel SOI-PDD design for the CEPC vertex detector

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Outline

- Pixel sensors for the vertex detector
  - Overview of R&D activities
- SOI-PDD structure
- CPV3 chip design
  - Diode optimization
  - Circuit description
  - Noise analysis
  - Test structures
- Perspectives on SOI-3D
- Summary

Detector Requirements

- Efficient tagging of heavy quarks (b/c) and τ leptons

→ impact parameter resolution

$$\sigma_{r\phi} = 5 \oplus \frac{10}{p(GeV)\sin^{3/2}\theta}\ (\mu m)$$

- Detector system requirements:
  - σ_{SP} near the IP: <3 μm → ~16μm pixel pitch
  - material budget: ≤ 0.15%X 0/layer
  - first layer located at a radius: ~1.6 cm
  - } power consumption <50mW/cm^2 , if air cooling used
  - pixel occupancy: <1 % → ~ μs level readout
- Radiation tolerance
- Time stamp: needed for short bunch spacing 25ns in Z^0 mode

Target:
fine pitch, low power, precise timing, fast pixel sensor + light structure

Beam-Induced Backgrounds (CDR)

- Detector occupancy <1%
  - assuming 10 μs readout interval, 16 um pixel pitch with a multiplicity of 9 per hit

Radiation level at the first vertex layer

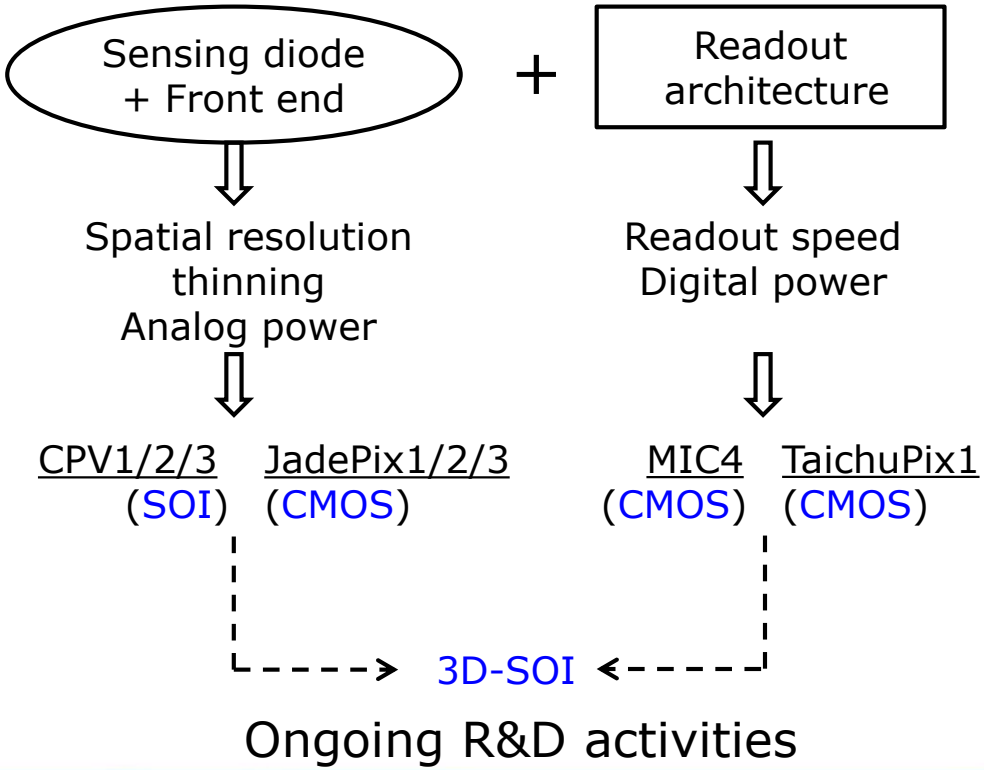
	H (240)	W (160)	Z (91)
Hit Density [hits/cm^2·BX]	2.4	2.3	0.25
TID [MRad/year]	0.93	2.9	3.4
NIEL [10^{12} 1 MeV n_{eq}/cm^2·year]	2.1	5.5	6.2

Occupancy at the first vertex layer

	H(240)	W(160)	Z(91)
Hit density (hits · cm^{-2} · BX^{-1})	2.4	2.3	0.25
Bunching spacing (μs)	0.68	0.21	0.025
Occupancy (%)	0.08	0.25	0.23

R&D activities on pixel sensors

- CMOS pixel sensor (CPS) - funded by MOST and IHEP
  - TowerJazz CiS 0.18 μm process
- SOI pixel sensor - funded by NSFC and IHEP
  - LAPIS 0.2 μm process



Ongoing R&D activities

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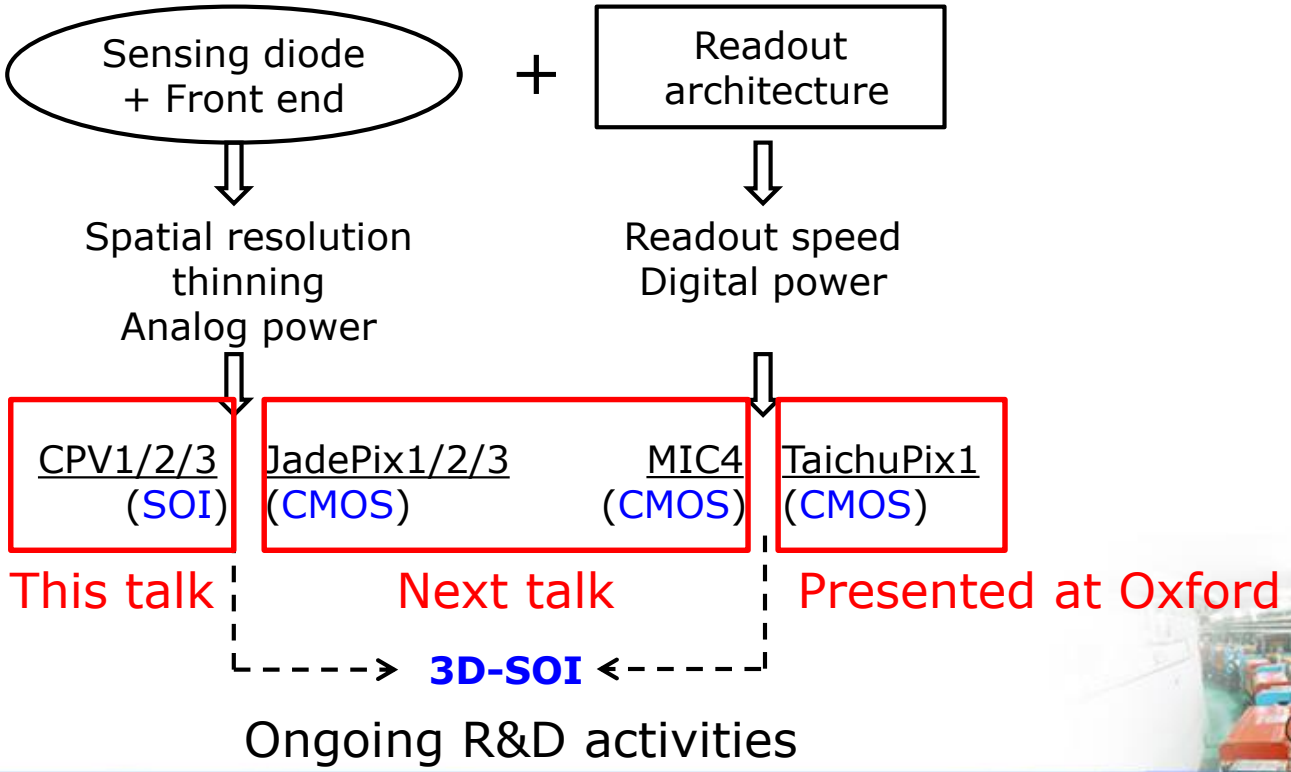
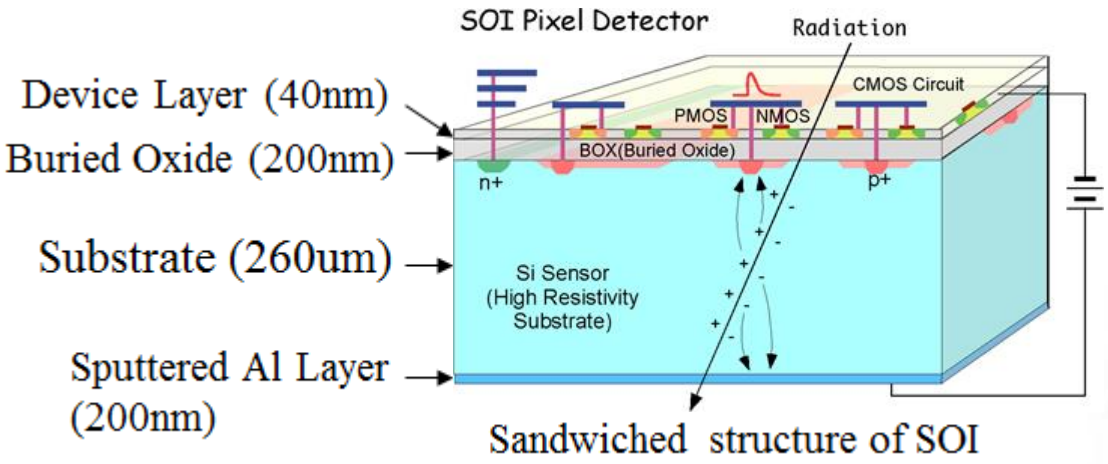


SOI pixel detector

- Sandwich structure
  - Upper: pixel circuit (device layer + 5 metal layers)
  - Middle: SiO_2 insulator with metallized through holes
  - Lower: diode array
- 0.2um FD-SOI CMOS process
  - High resistive substrate
  - Low-power optimized
  - No latch-up and very low Single Event Effect

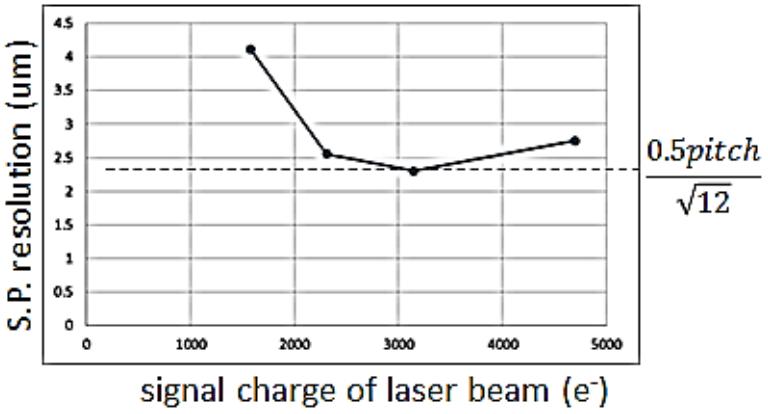


Evolution of SOI detector process

- Pinned Depleted Diode (PDD)
  - CPV3 chip design
- Double-SOI
  - CPV1/CPV2 chip design
- Nested-wells
- Buried P-Well (BPW)

- CPV2 performance
  - Thinned down to 75um thick
  - Temporal noise 6e-
  - Residual of laser positon 2.3um (σ)

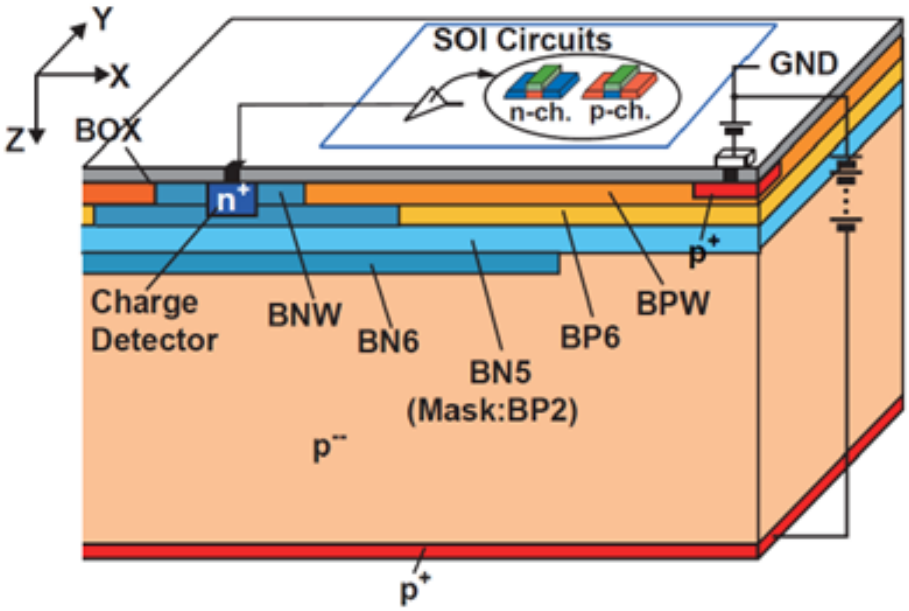
Ref: 1. Y. Lu, FEE2018, May 2018
2. Z. Wu, et al, NIMA924 (2019) 409–416

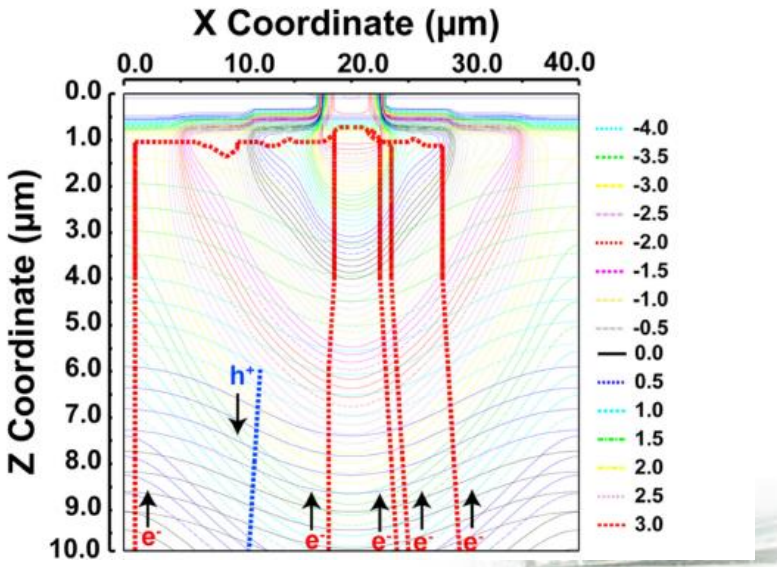


- Excessive FPN noise 114e-
  - To be reduced < 20e-

A conceptual view of PDD

- Proposed by Shoji Kawahito (Shizuoka U.)
  - Pinned Si surface layer → reduction of surface leakage by 2 orders
  - Depleted charge collection electrode → reduction of diode capacitance
  - Lateral electric field → improved charge collection efficiency

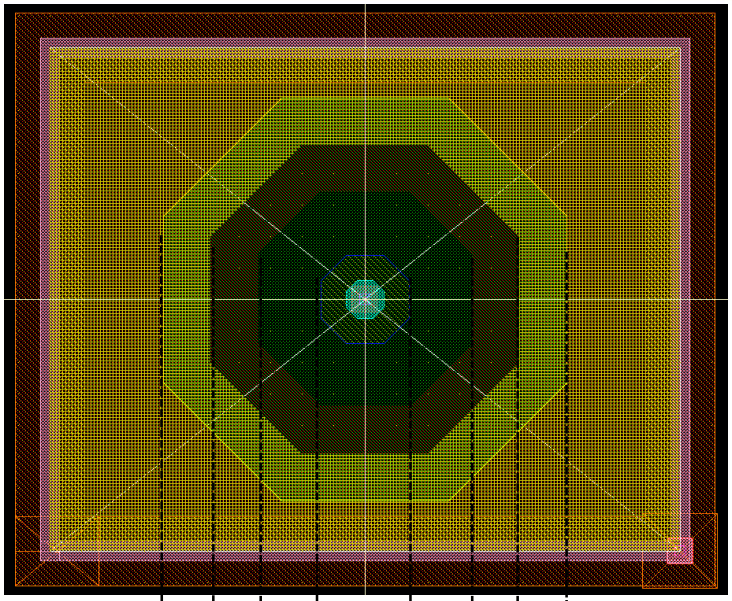


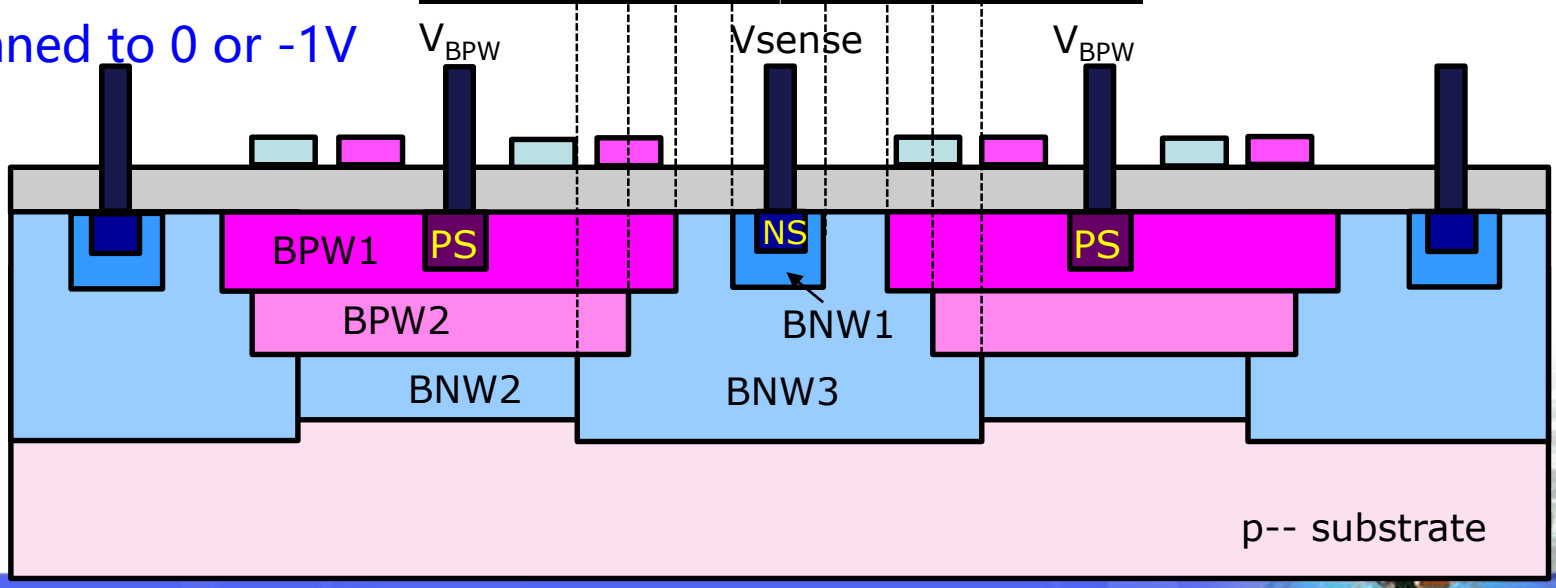


Ref: Sensors 2018, 18, 27; doi:10.3390/s18010027

Stackup of pixel layers in CPV3

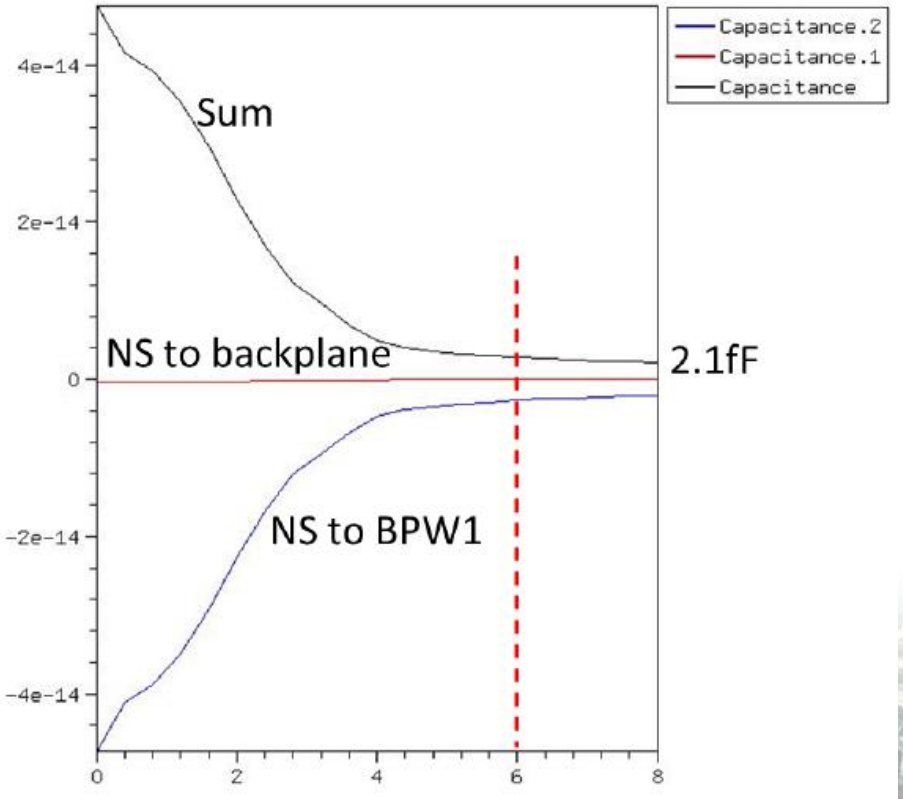
- HR P-type substrate
  - 25 KΩ·cm
  - Reverse biased > -10V
- NS and BNW1/2/3
  - Charge collection
  - Positive V_{sense}
- PS and BPW1/2
  - V_{BPW} Pinned to 0 or -1V





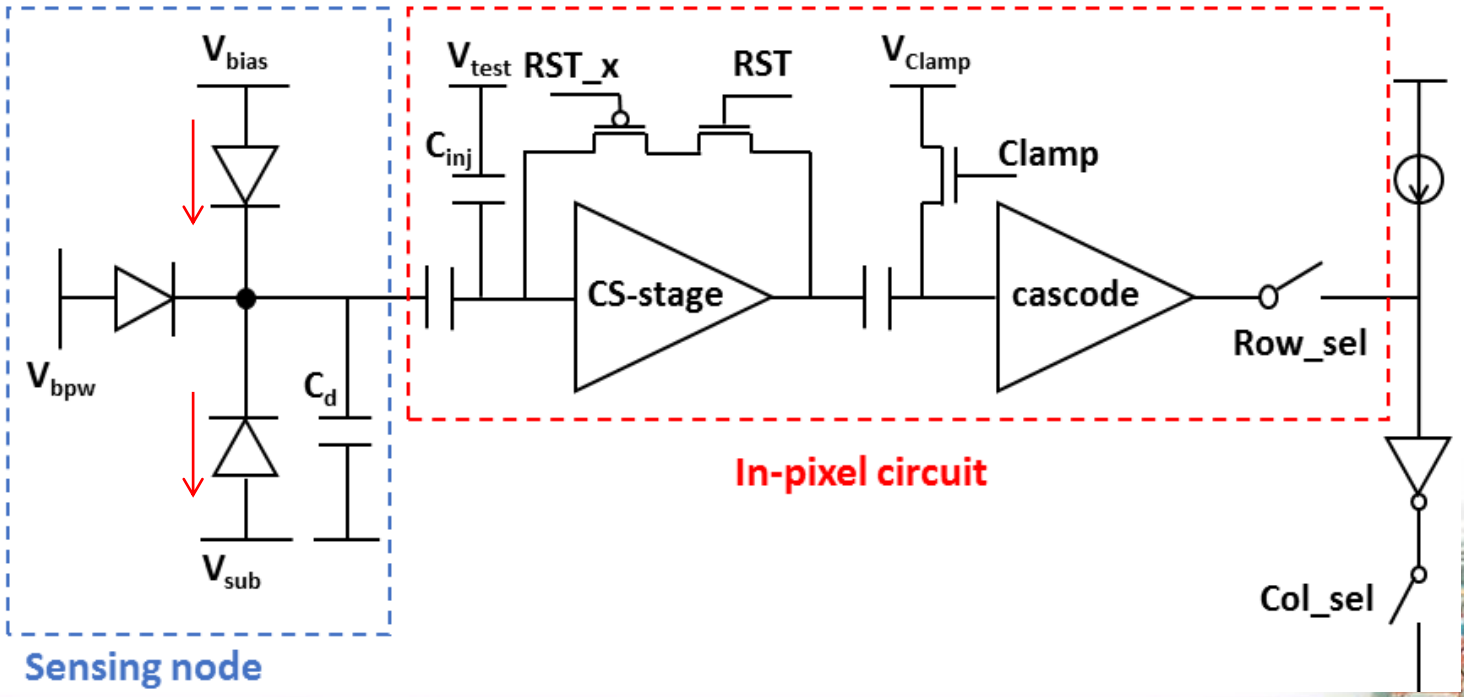
Diode optimization

- Pixel pitch 16 um * 20 um
  - Minimum size to accommodate the pixel circuit
- Capacitance optimization
  - NS to BPW1 dominates
  - Reverse bias > 6V is required
  - 2 um of the spacing between BNW1 and BPW1 is chosen



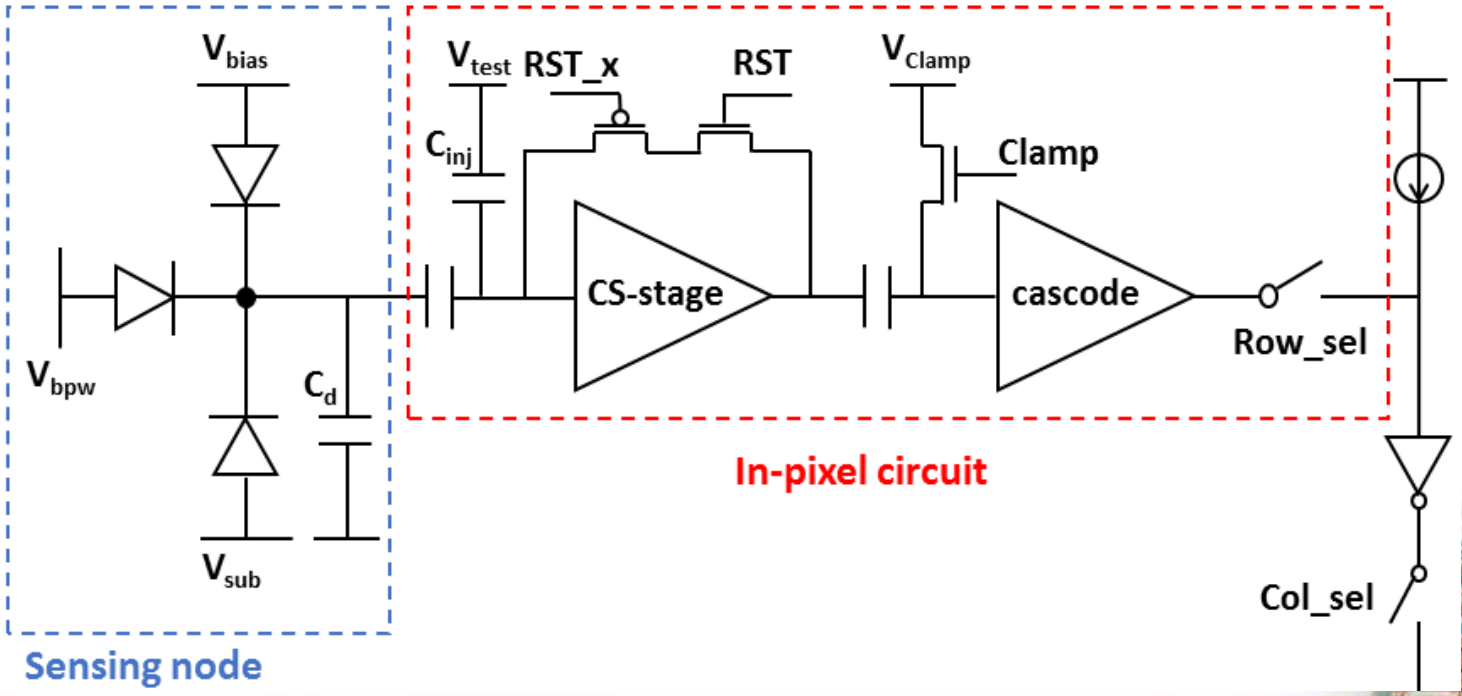
Bias of sensing node

- Sensing node AC-coupled to the amplifier for low capacitance
  - Voltage on the sensing node is set by V_{bias}
  - MIM capacitor to allow V_{bias} up to +10V
  - Leakage current around 100 fA/pixel thanks to the PDD structure
  - 2% loss of signal over 100 us integration time



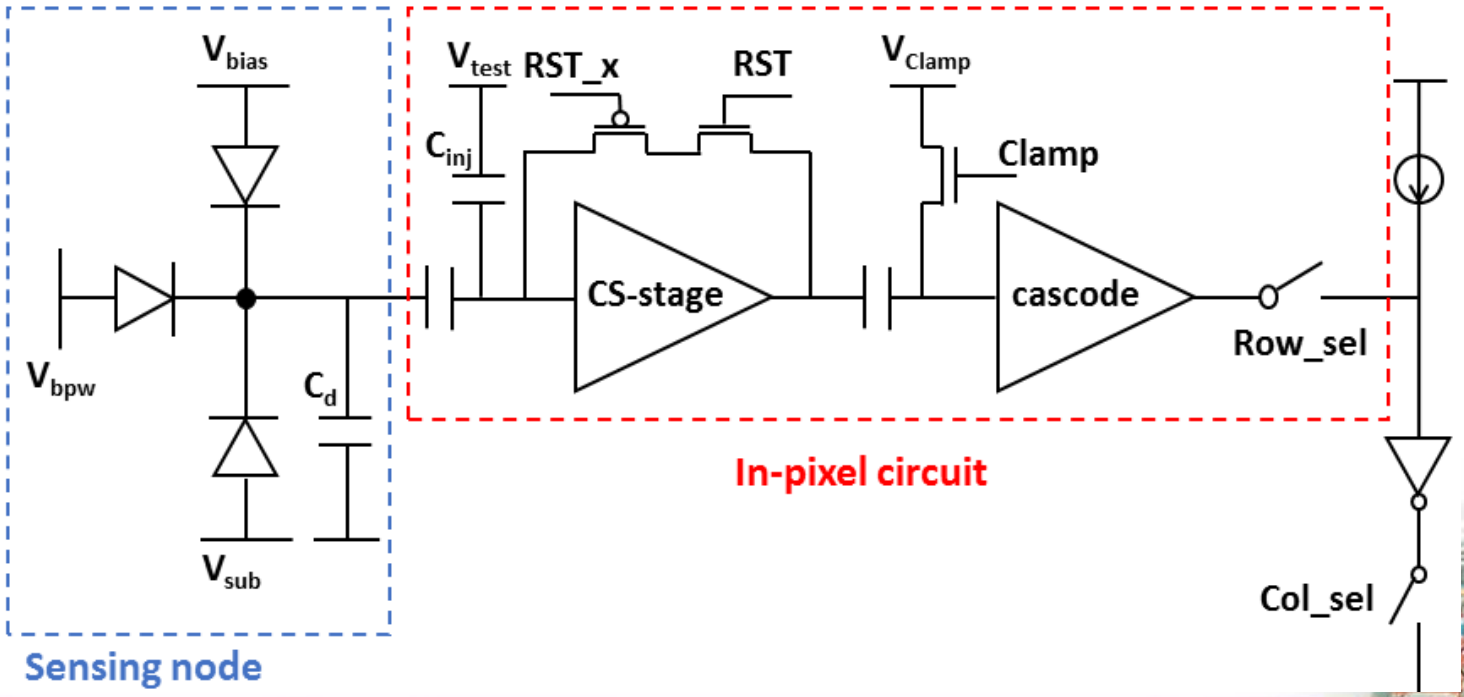
Amplifier

- Common Source (CS) amplifier, 1st stage
  - DC gain ~13
  - 1 uA consumed only when readout (rolling shutter mode, < 1% duty cycle)
  - Forced to initial state after readout by a pair of complementary reset transistors
  - C_{inj} = 0.27fF for electrical pulse test



Discriminator

- Cascode amplifier, 2nd stage
  - Correlated Double Sampling (CDS) to reduce KTC noise
  - Cascode input with its active load shared on the column line
  - 4 uA consumed only when readout (rolling shutter mode, < 1% duty cycle)
  - Intrinsic threshold 525mV, adjustable by V_{clamp}



Noise analysis

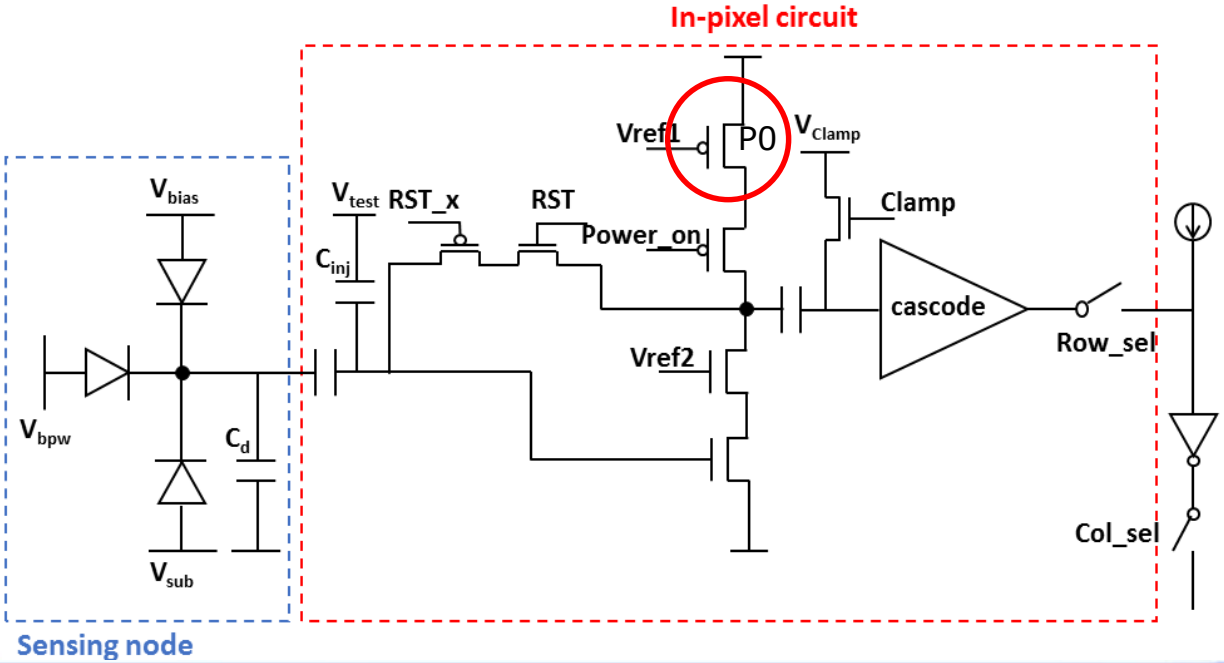
- Temporal Noise (TN)
  - Shot noise is negligible due to low leakage current
  - Thermal noise is the dominant component
  - 6 e^- achieved on CPV2 design
- Fixed Pattern Noise (FPN)
  - Excessive FPN has been an issue in CPV2 design
  - W/L = 0.63/0.2 um for the input Tr. of 1st stage
  - W/L = 2.4/0.2 um for the input Tr. of 2nd stage
  - Process variation added to the HSPICE model and qualified with CPV2 results.

$$\sigma(\mathrm{W}) \propto \frac{1}{\sqrt{L}}, \sigma(L) \propto \frac{1}{\sqrt{W}}, \sigma(\mathrm{Vth}) \propto \frac{1}{\sqrt{LW}}, \sigma(\mathrm{Tox}) \propto \frac{1}{\sqrt{LW}}$$

  - Statistical simulation, FPN = 12 e^-

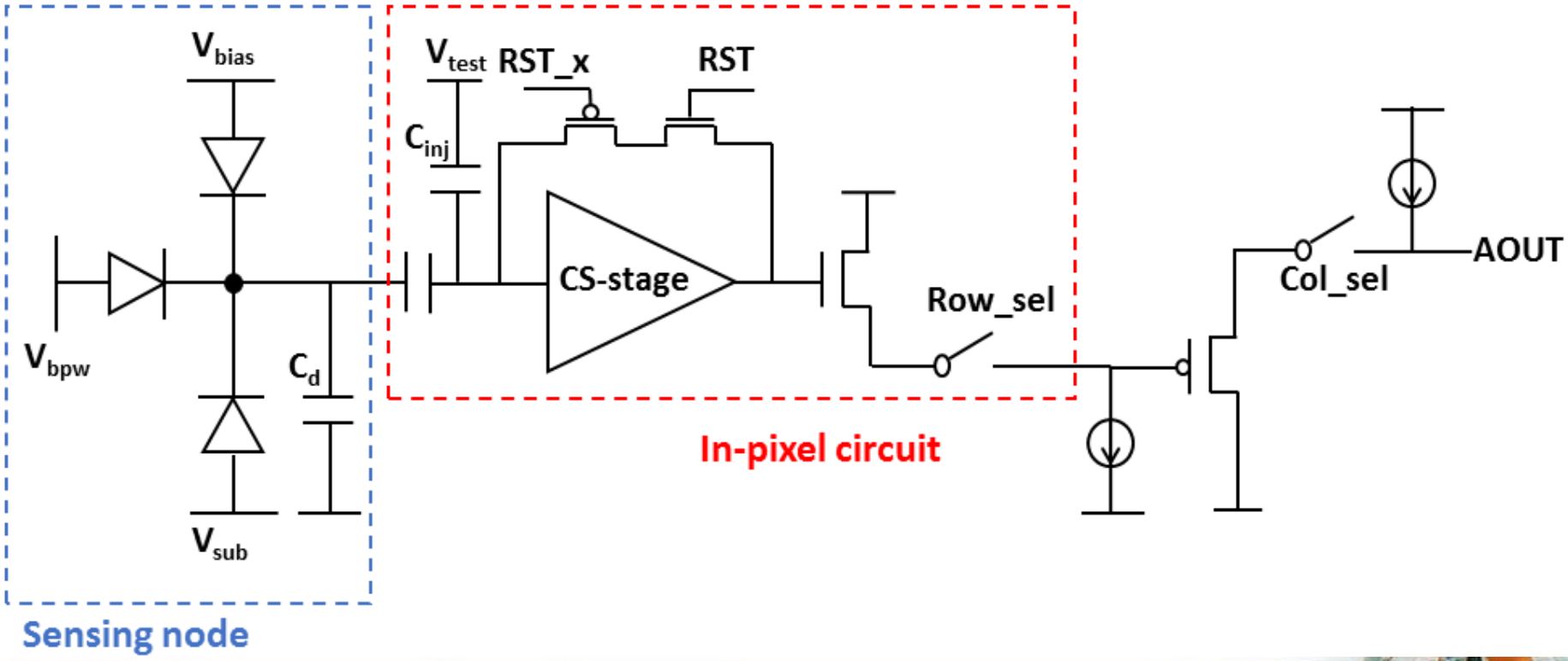
Test structure 1: cascode 1st stage

- CS-stage of the amplifier replaced by a cascode stage
  - To mitigate the miller effect and to improve the CVF
  - Carefully tuned to have a DC gain < 30 (for a proper dynamic range)
- Optimized the size of P0 Transistor (as the active load)
  - W/L = 2/0.3 um for lower FPN, DC gain = 25
  - W/L = 0.63/0.3 um for lower TN, DC gain =30



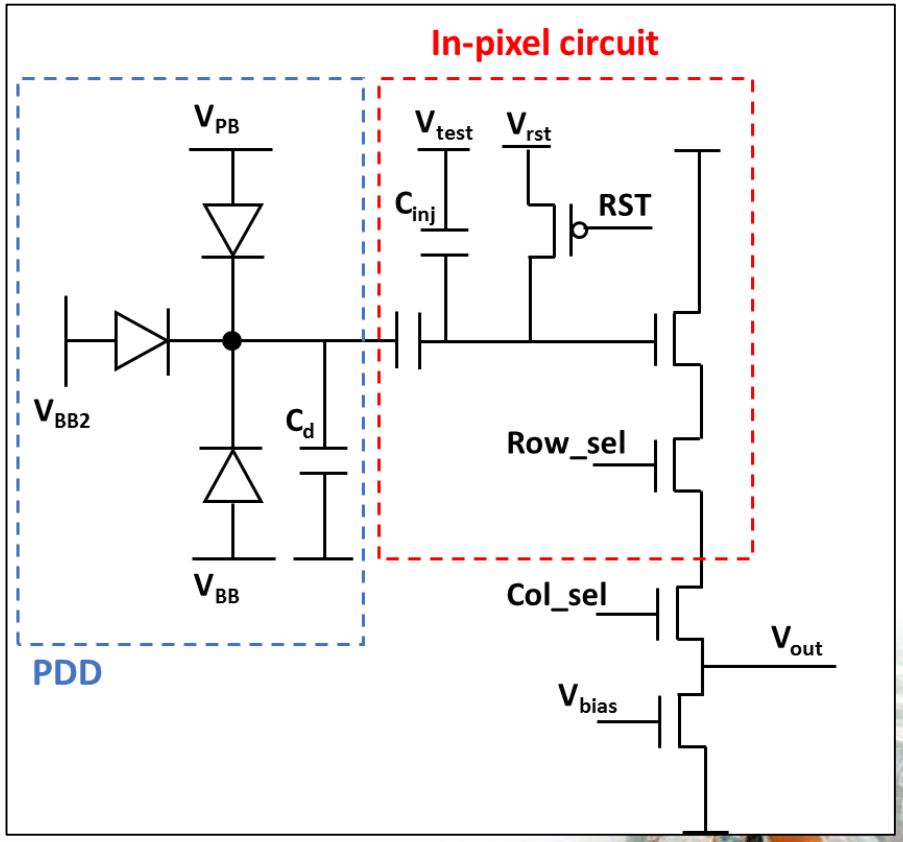
Test structure 2: analog output

- Discriminator replaced with a source follower for analog output
  - To make the output of CS-stage accessible during test
  - A powerful tool to investigate possible malfunction of CS-stage



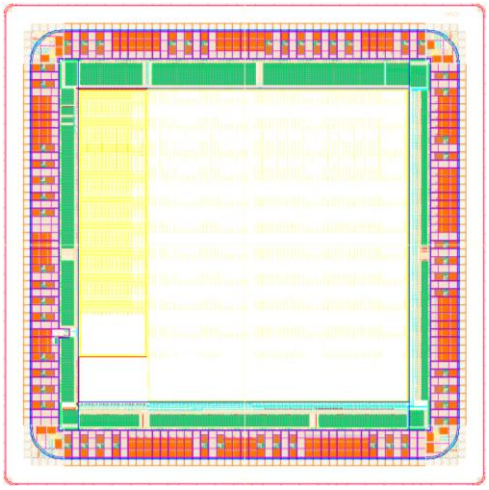
Test structure 3: 3-Transistor readout

- A 3-Transistor source follower used to read out the PDD sensing node
  - Large dynamic range to characterize the PDD sensor
  - Simple and straightforward



Status of CPV3

- Submitted in Feb. 2019
  - First trial on the PDD structure
  - Dedicated bias scheme to minimize capacitance
  - Optimized for low FPN 12e$^-$
  - Pixel matrix divided as 45 regions, to verify design options
  - Mask area: 6mm×6mm
- Testing system is ready
  - Sub-board, FPGA board, DAQ
  - To be wire-bonded and testing…



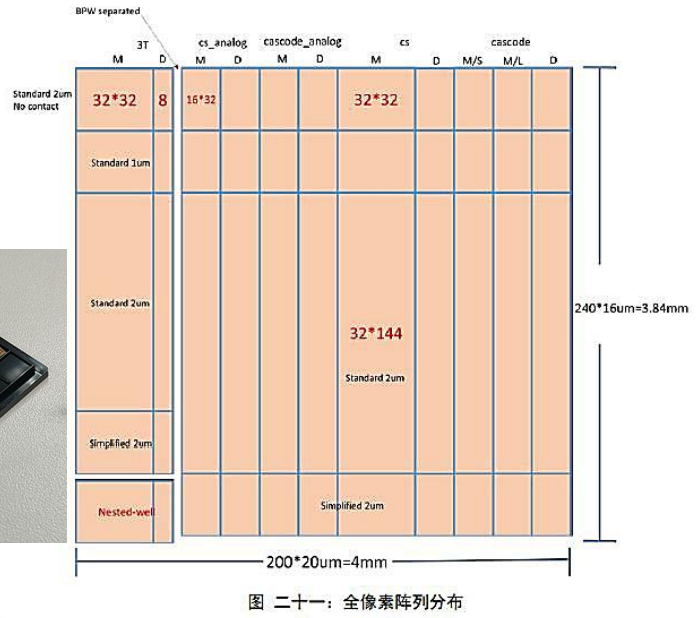
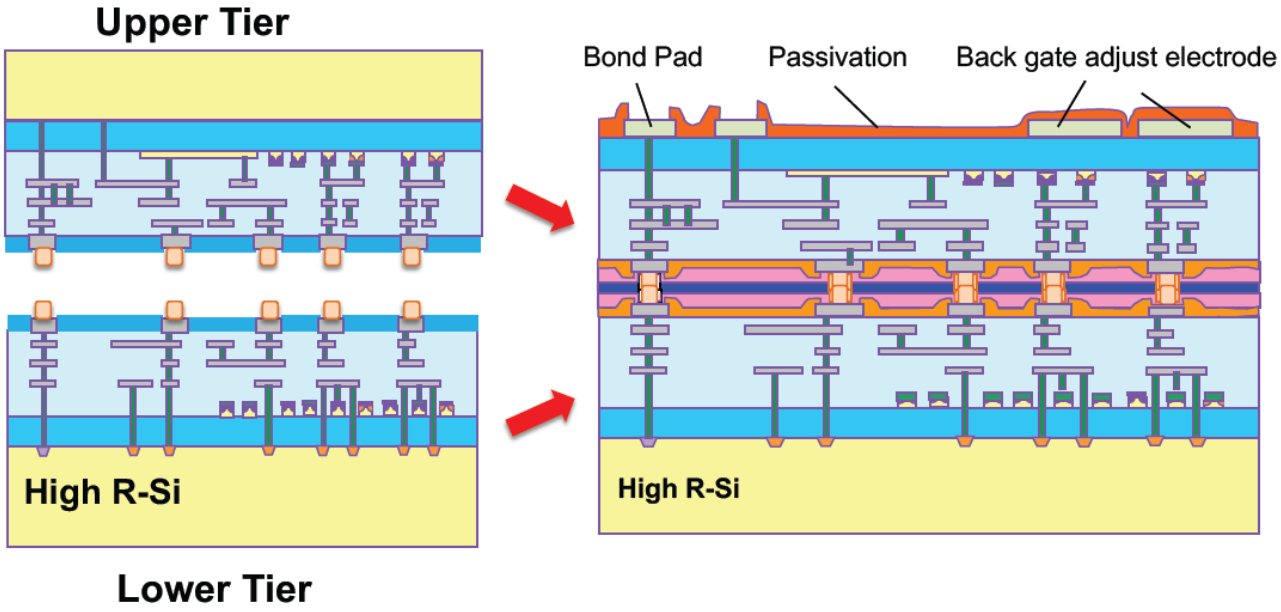


图 二十一：全像素阵列分布

Perspectives on SOI-3D

- A 5-year proposal granted by the NSFC this year
- SOI wafers greatly simplify 3D integration
  - The lower tier can be either SOI or CMOS pixel sensor
- SOI-3D has been demonstrated by the SOFIST4 3D chip for ILC
  - 10k connections in single chip yields 99.98%
  - images of the β-ray tracks of ^{90}Sr

Ref:
M. Yamada, IEEE 3DIC, Oct. 8th, Sendai, Japan, 2019



Summary

- Requirements of CEPC vertex detector is unprecedented
  - CPV1/2/3 are targeting on the spatial resolution, low power consumption and modest readout speed
- CPV3 has been adapted to the PDD structure and optimized for low FPN
  - A variety of design options to be verified on this design
- SOI-3D is bringing about a new dimension of design freedom
  - Additional circuit layer with the material slightly increased by 10 um
  - Compatible with both SOI and CMOS pixel sensors

Acknowledgements

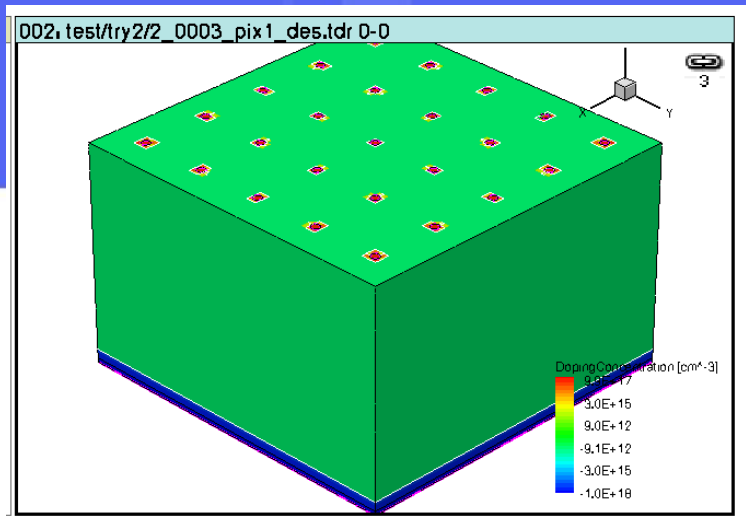
- This work is supported by the National Nature Science Foundation of China, Grant 11575220.
- And the CAS Center for Excellence in Particle Physics (CCEPP)

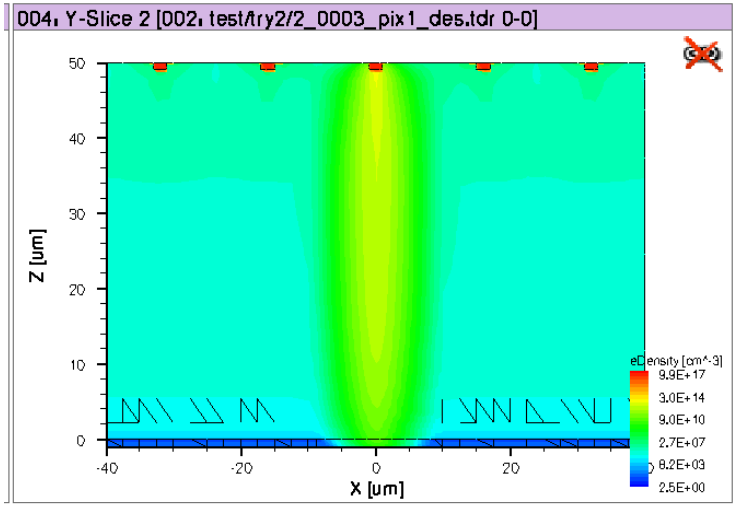
- Backup slides

Device simulation

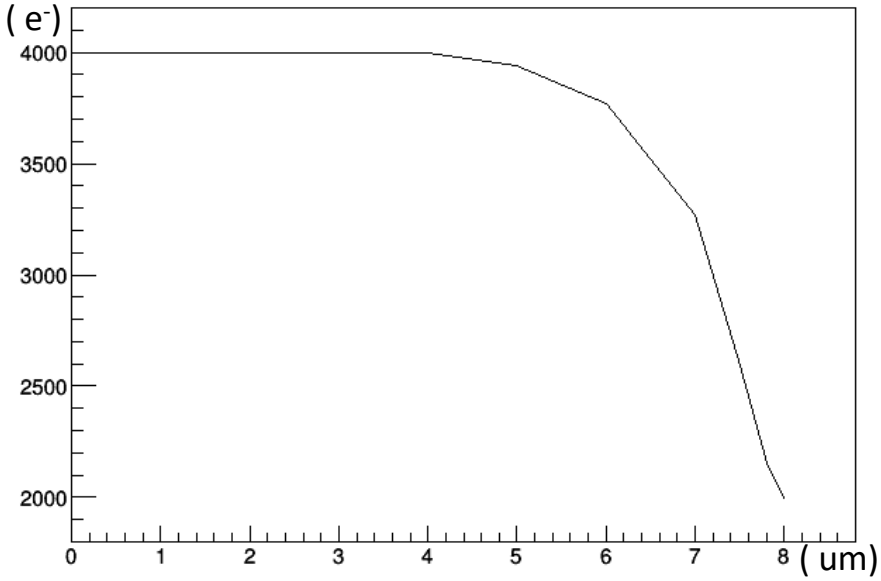
How to achieve s.p. resolution < 3um?

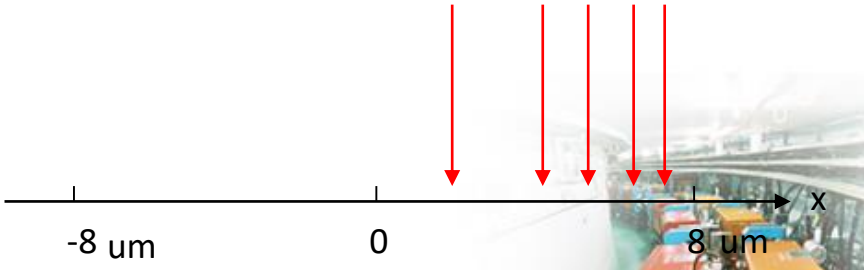
- Device configuration
  - HR P substrate, N electrode
  - Pixel pitch 16um
  - Sensor thickness 50um
- Transport of charge carriers
  - Analyzed by TCAD tools





Collected charge vs hit position

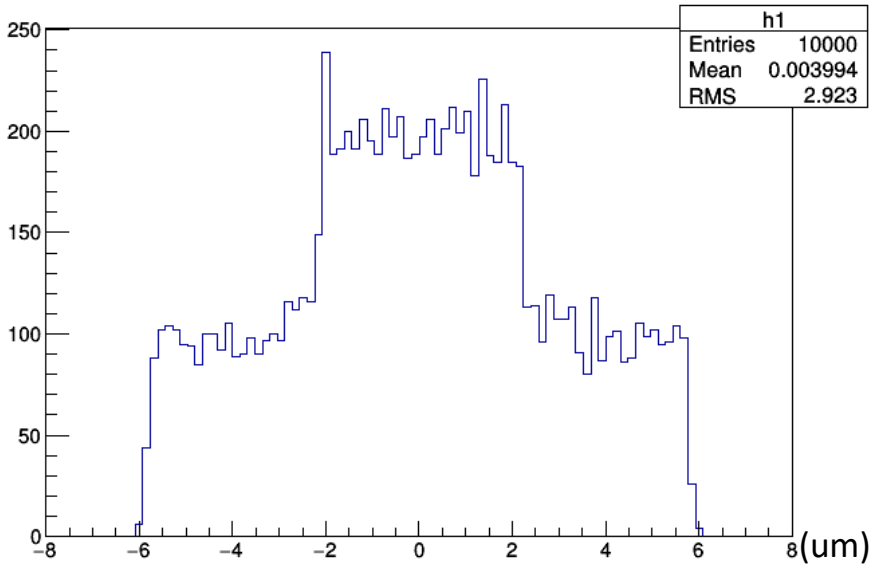




Device simulation

- Low noise front-end is critical to make use of the charge sharing effect
  - ENC ~ 20e$^-$
  - Threshold ~ 200e$^-$
- Limitation of 1D approach
  - Corner of square pixel

Residual distribution with threshold at 200e-



Single point resolution vs threshold