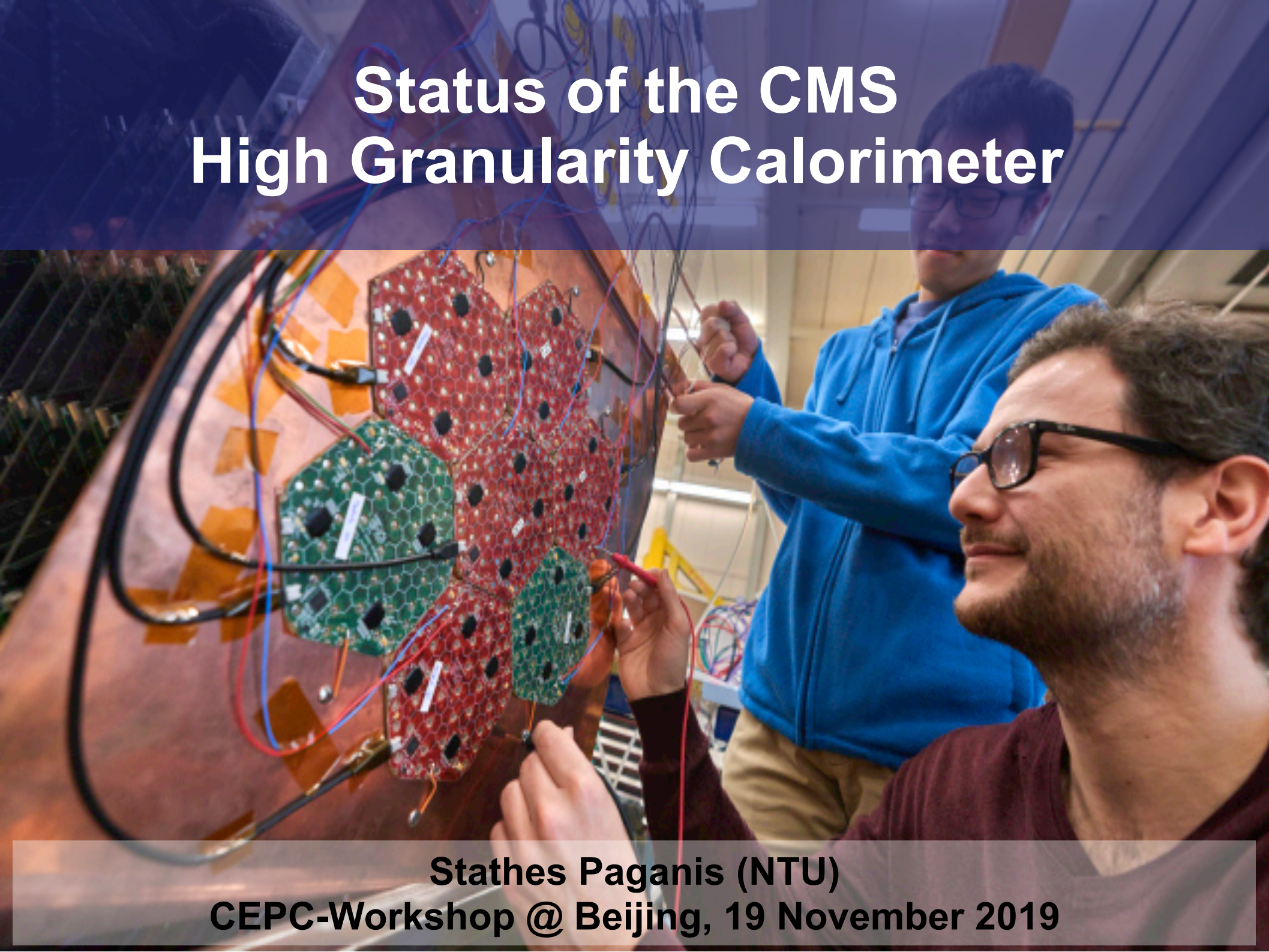
Status of the CMS High Granularity Calorimeter



Stathes Paganis (NTU)

CEPC-Workshop @ Beijing, 19 November 2019

Phase II: High Luminosity LHC

- HL-LHC: expected to deliver 10x the luminosity delivered in Phase I

- CMS upgrade
  - Increased acceptance: tracker ($|\eta|=4$) and muon spectrometer ($|\eta|=2.8$)
  - Higher first level trigger (L1) rate: 100kHz → 750kHz
    - to maintain comparable trigger performance at higher pileup
  - L1 trigger latency 3.4μs → 12.5μs
    - to provide time for the new track-based hardware trigger

CMS High Granularity Calorimeter

Key Parameters (updated from the TDR):

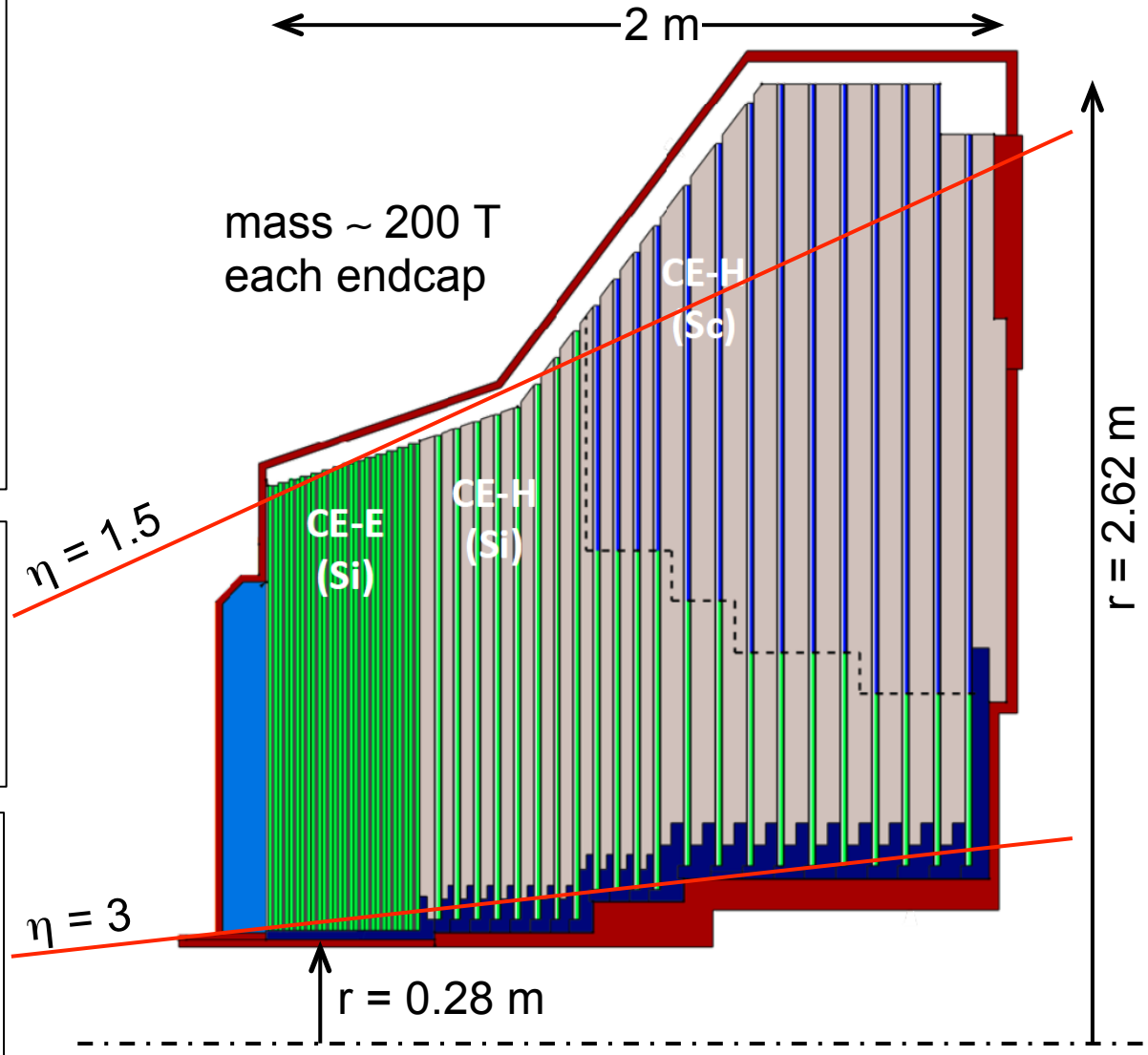
- HGCAL covers $1.5 < \eta < 3.0$
- **Full system maintained at -30°C**
- **~640 m²** of silicon sensors
- **~370 m²** of scintillators
- 6.1M Si channels, 0.5 or 1.1 cm² cell size
  240k scintillator-tile channels (η-ϕ)
  - Data readout from all layers
  - Trigger readout from alternate layers in CE-E and all in CE-H
- ~31000 Si modules (incl. spares)

Active Elements:

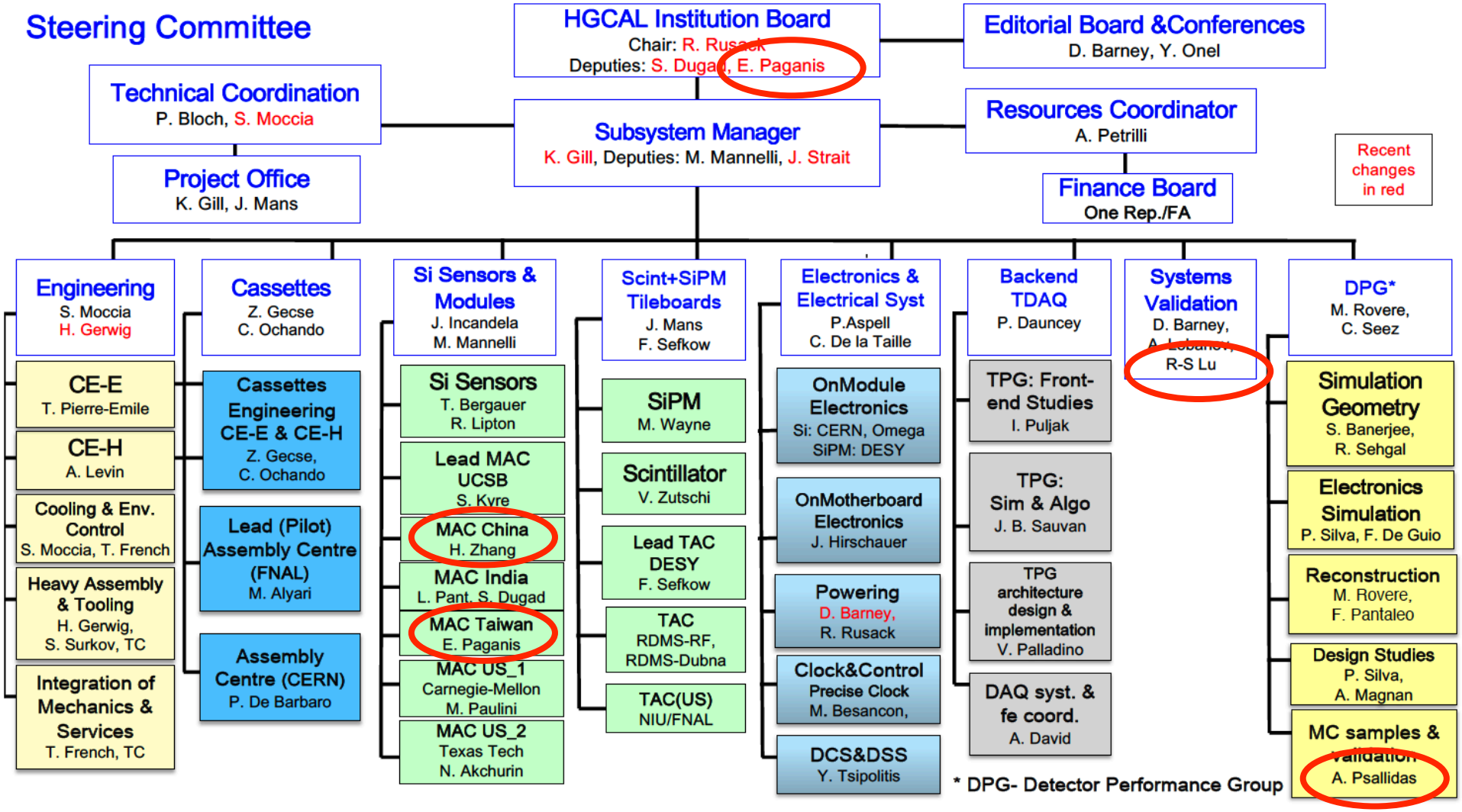
- Si sensors (full and partial hexagons) in CE-E and high-radiation region of CE-H.
- SiPM-on-Scintillating tiles in low-radiation region of CE-H

Electromagnetic calorimeter (**CE-E**): **Si**, Cu/CuW/Pb absorbers, 28 layers, 25.5 X_0

Hadronic calorimeter (**CE-H**): **Si** & **scintillator**, steel absorbers, 22 layers, ~9.5λ (including CE-E)



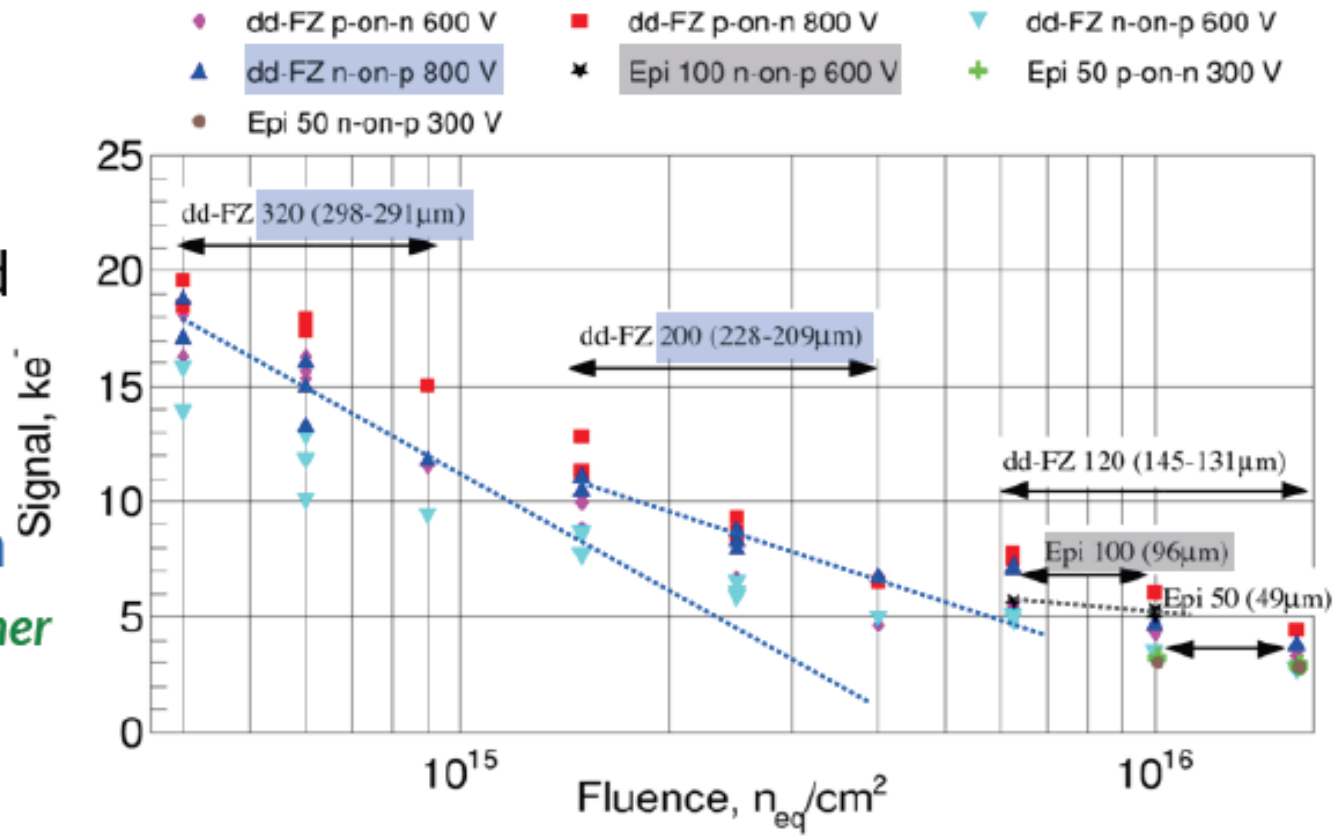
Project Organization (2019)

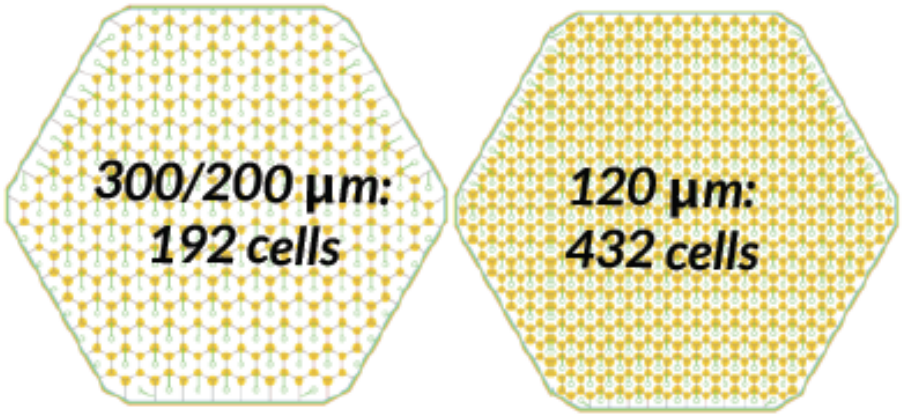


Sensors

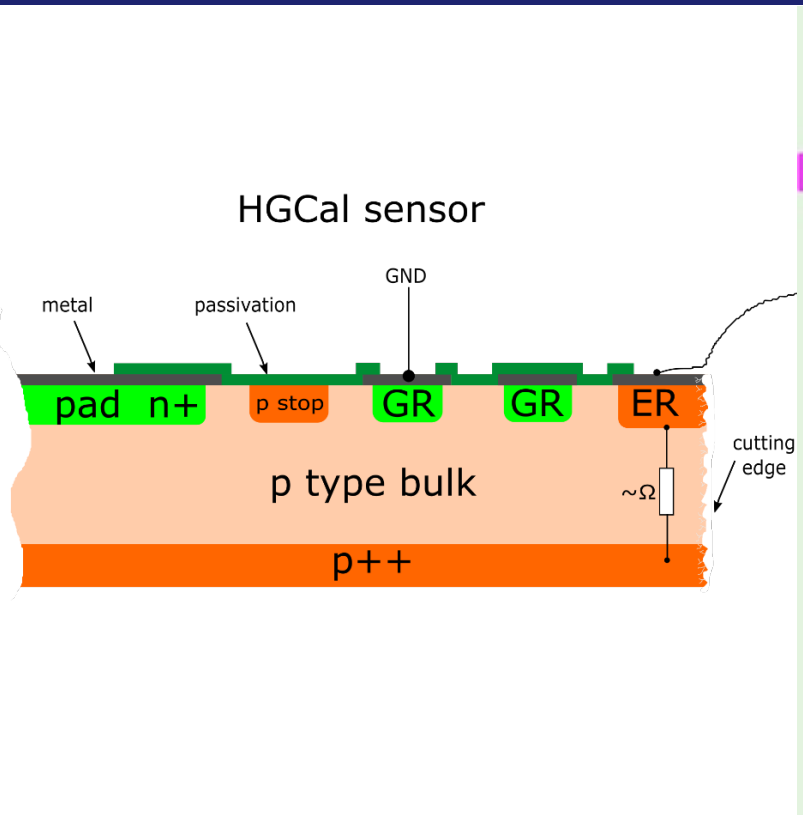
HGCAL Silicon sensors

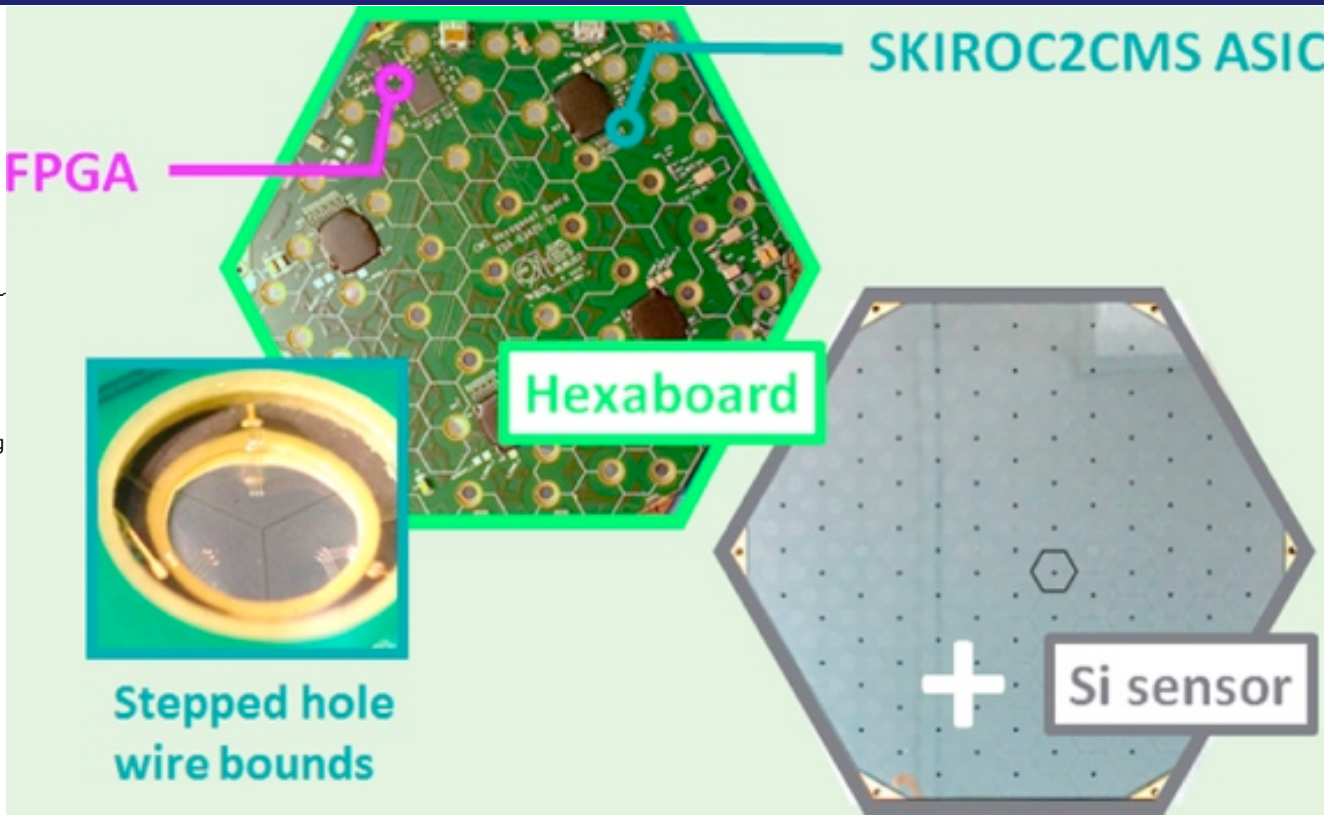
- 8 inch wafers
- Hexagonal sensor geometry
- Planar p-type DC-coupled sensor pads
- Active thickness:
  300 µm, 200 µm, 120 µm
  - ***Advantage of deploying thinner sensors in the higher fluence regions***
    - ***More tolerant to large neutron fluences***
  - ***Reduced cell size in thinner sensors***
    - ***Keeping the capacitance reasonable***

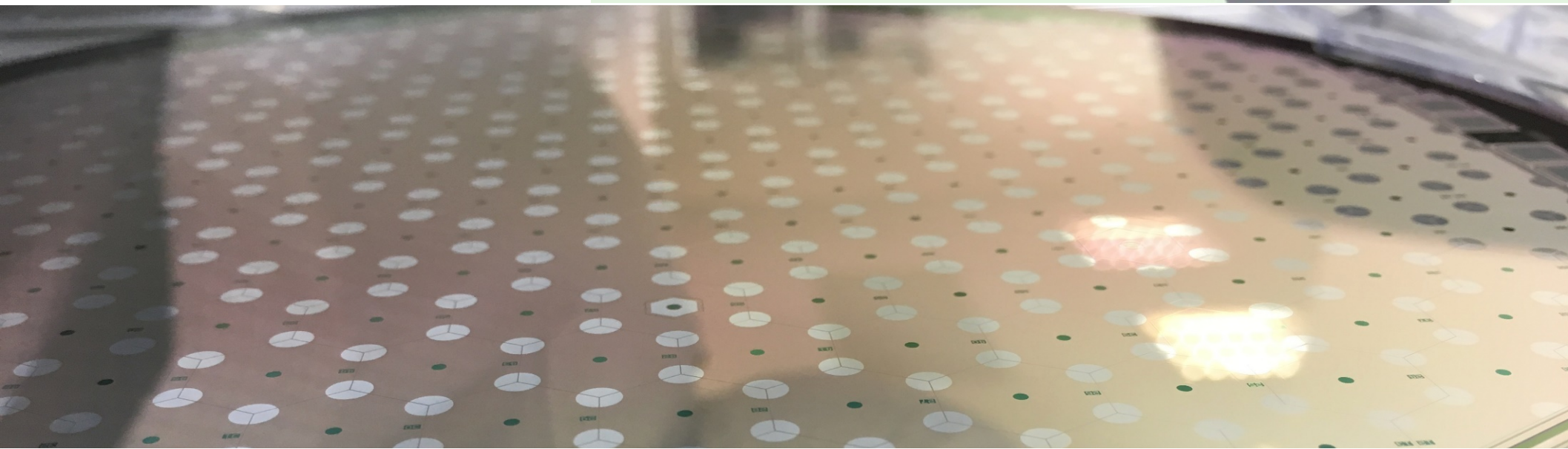




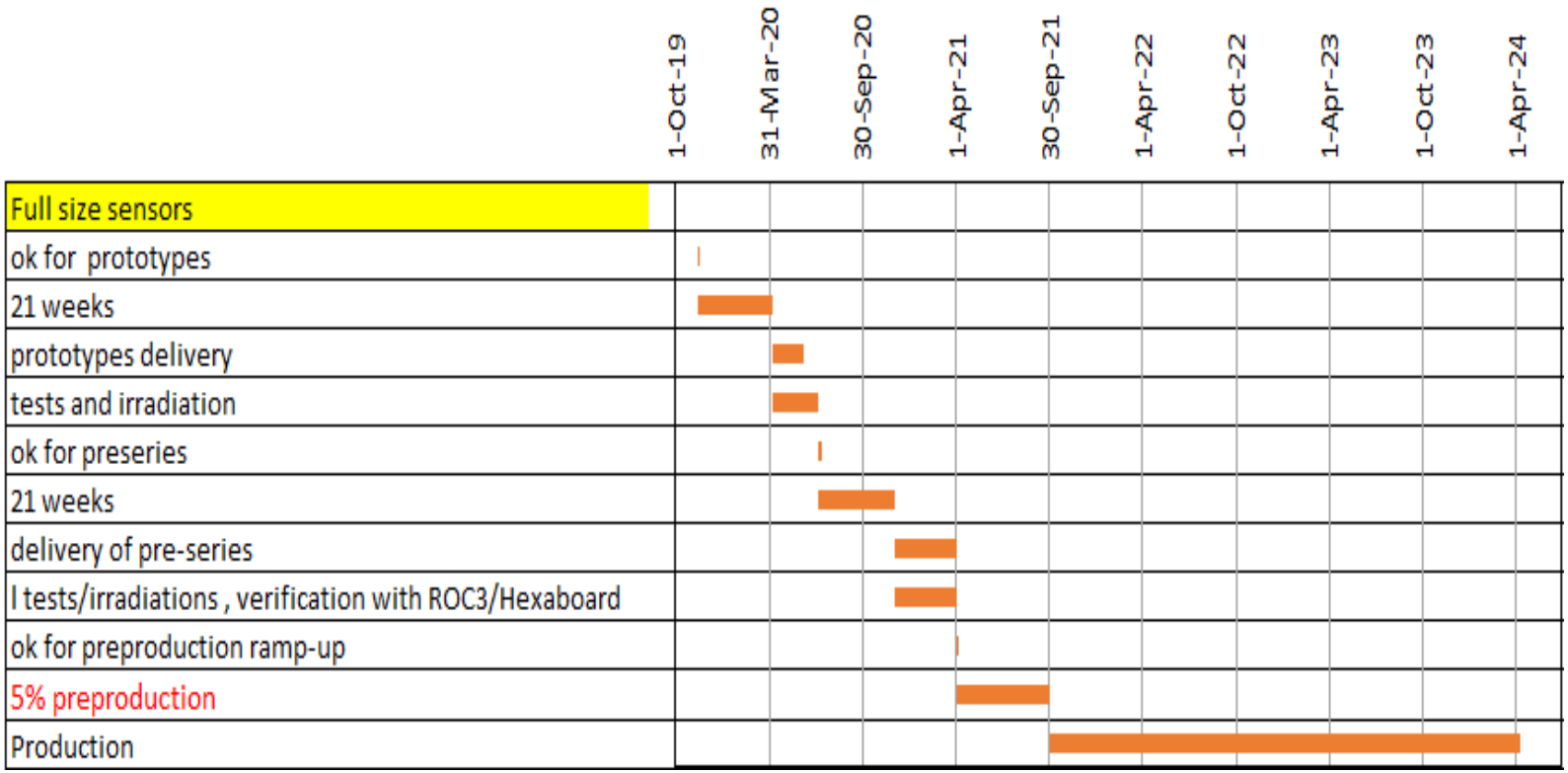
HGCAL Sensor and Hexaboard







Silicon sensor production schedule



- Design changes for front-side sensor bias (due to backplane fragility mitigation)
  - Preparations for oxide quality improvement on HPK 8” line ongoing
- As things stand, the last sensor delivery would slide from Q4 2023 to Q1 2024
  - Discussion ongoing with HPK to reduce production lead times.

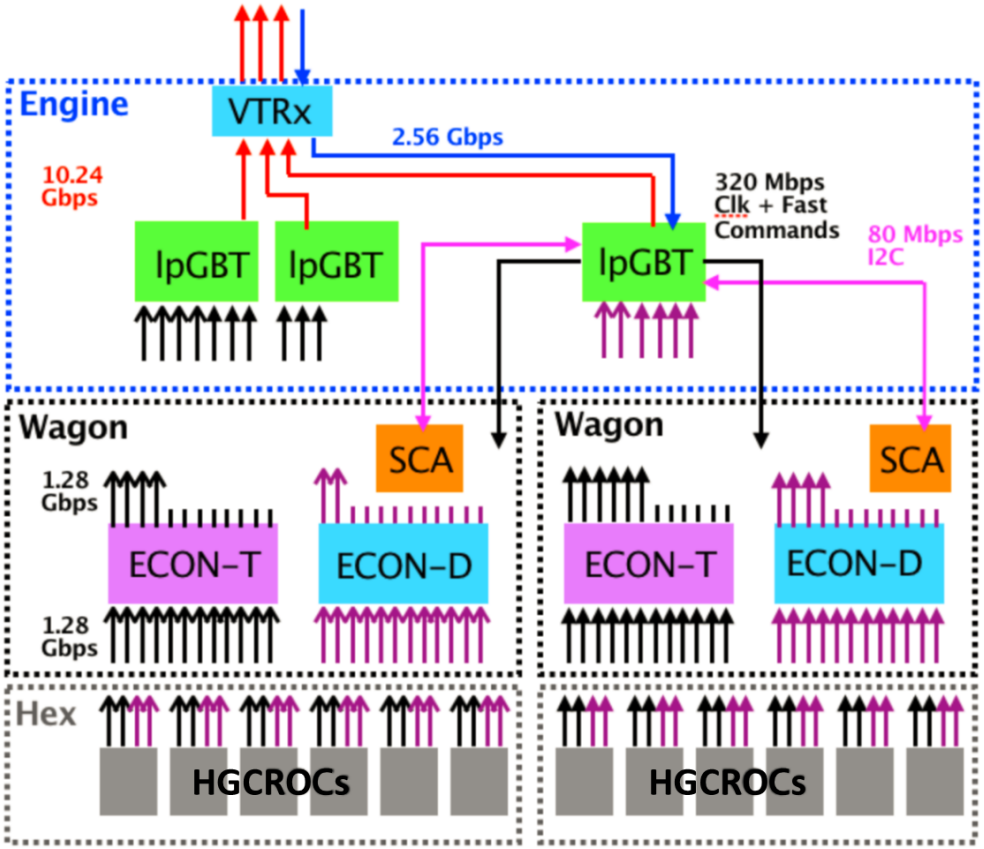
Electronics

FEE Architecture

Two data paths:

40 MHz trigger data: ECON-T aggregates, selects/compresses, serializes, and transmits to lpGBT

750kHz DAQ data: On L1 accept, ECON-D applies zero suppression, aggregates, serializes, and transmits to lpGBT



HGCAL specific:
HGCROC
ECON
Hexaboard
Motherboard (Engine and Wagon)

Common Project:
lpGBT
VTRX+
SCA
(also FEAST, BPOL)

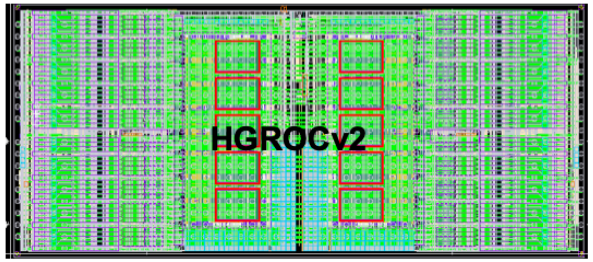
SKIROC2_CMS ASIC for initial system prototypes & test-beam
SiGe, analog with TOT
Tape-out Jan. 2016, TWEPP 2016

TV1 & 2 Test vehicles
130nm CMOS, TV1 preamplifier studies, TV2 analog channel
Tape-out 2016, TV2 in TWEPP 2017

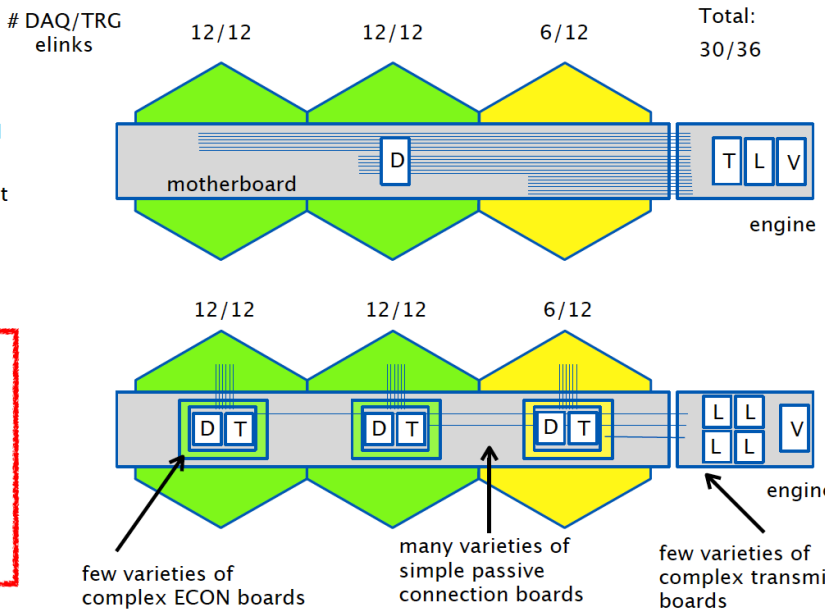
HGCROC-V1 Designed, fabricated & tested
130nm CMOS,
Tape-out July 2017, TWEPP 2018, Fully tested.

HGCROC-V2 Designed, fabricated & under test
130nm CMOS
Tape-out Feb. 2019, received end-June
Naked and packaged chip tests ongoing

HGCROC-V3 Currently in the design phase
130nm CMOS
Tape-out due Feb. 2020



FEE Integration



Details :

- ECON boards would also hold SCA and clock fanout
- Signals run both directions : data ➔ , ⬅ clock/control

Advantages / Disadvantages of two approaches

	Centralized 36x1G in (3/1)x10G out	**Decentralized** 12x1G in 12x1G out

Advantages	• Less dense 2-chip engine
	• more flexible load balancing
	• transmitter redundancy
	• ~25% lower power
		• More naturally allows isolation of complexity into
		  • ECON board
		  • Transmitter board
		• More unified ECON-D / ECON-T architectures
		• Less ECON design time, lower risk of ECON prototype problems
		• Naturally accommodates FPGA ECON emulator board for early system prototyping
		• Simpler / less expensive ECON package
		• decentralization lowers single point failure risk

Disadvantages	• Longer ECON design time • Higher risk of ECON prototype problems • Single point failure	• More dense 4-chip engine • Less flexible load balancing

FEE Integration

Progressing coherently on details of the front-end electronics integration.

Motherboards implemented as “engine & wagons” compatible with the decentralized architecture

Engine:

Hosts the lpGBT and VTRX+ optical components

Small and complex board, with fine-pitch components.

Aiming for few variants

Wagon:

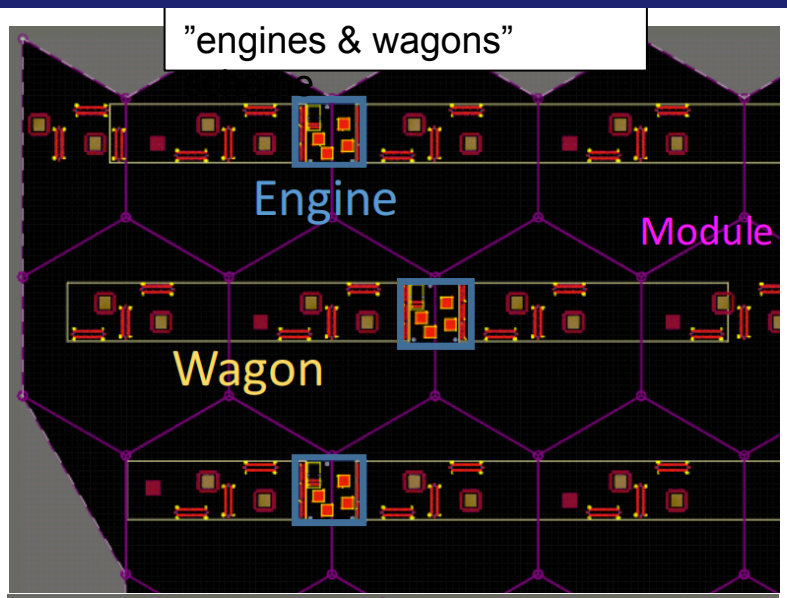
Hosts slow control chip (GBT-SCA).

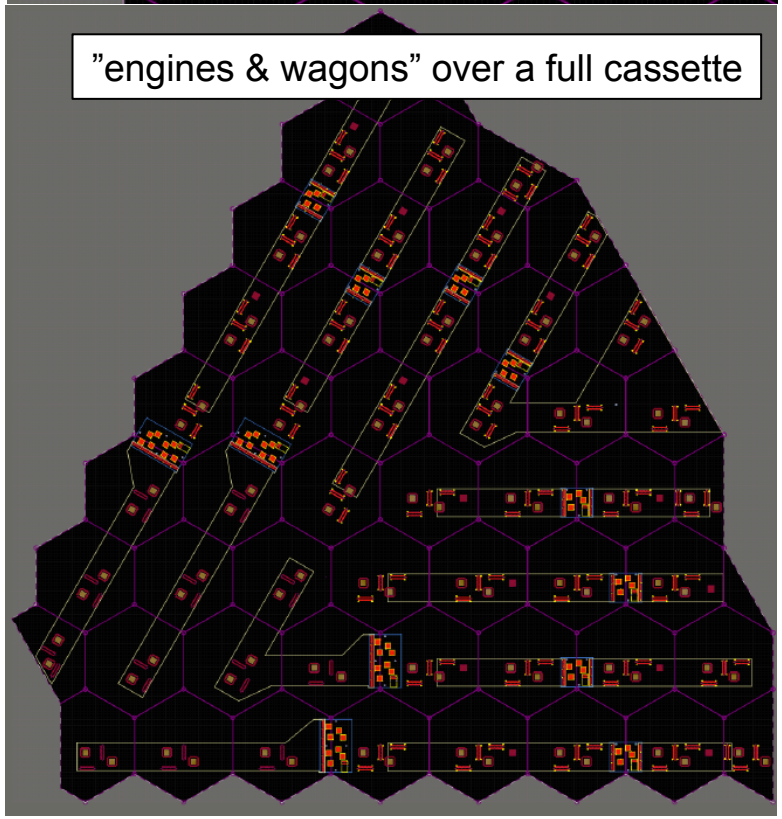
Up to 2 wagons per engine, spanning up to 3 modules each

Larger, but much simpler board

Multiple (15+) wagon designs needed to cover the radial geometry

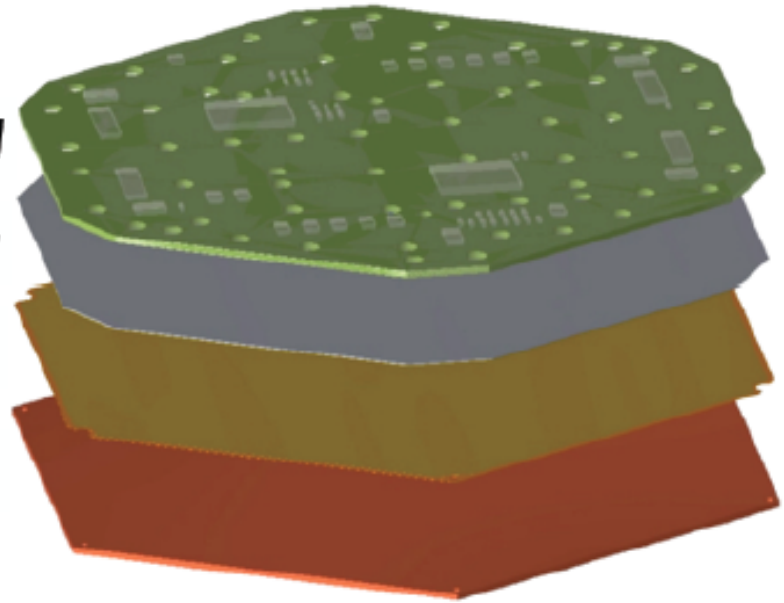
ECONs mounted on simple mezzanines in the low density region, and on the wagon in high density region

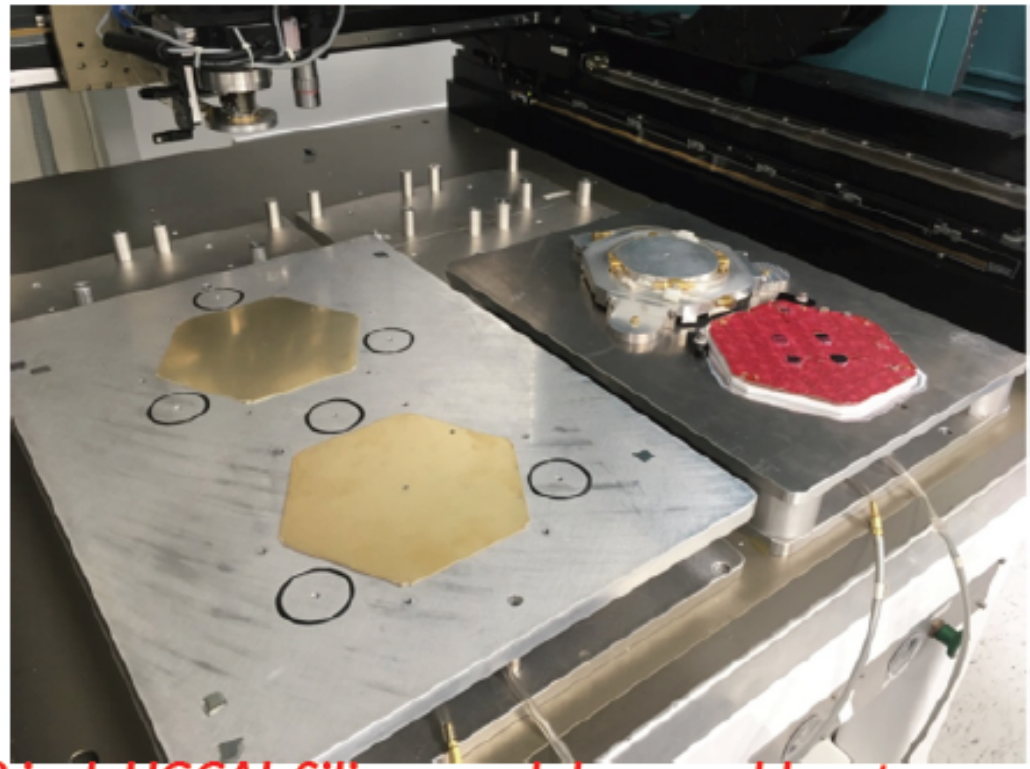




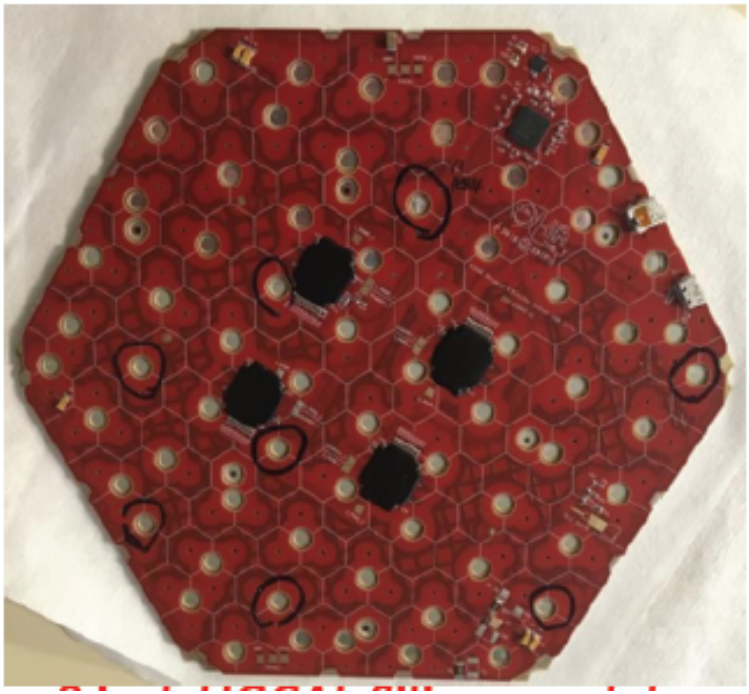
Modules

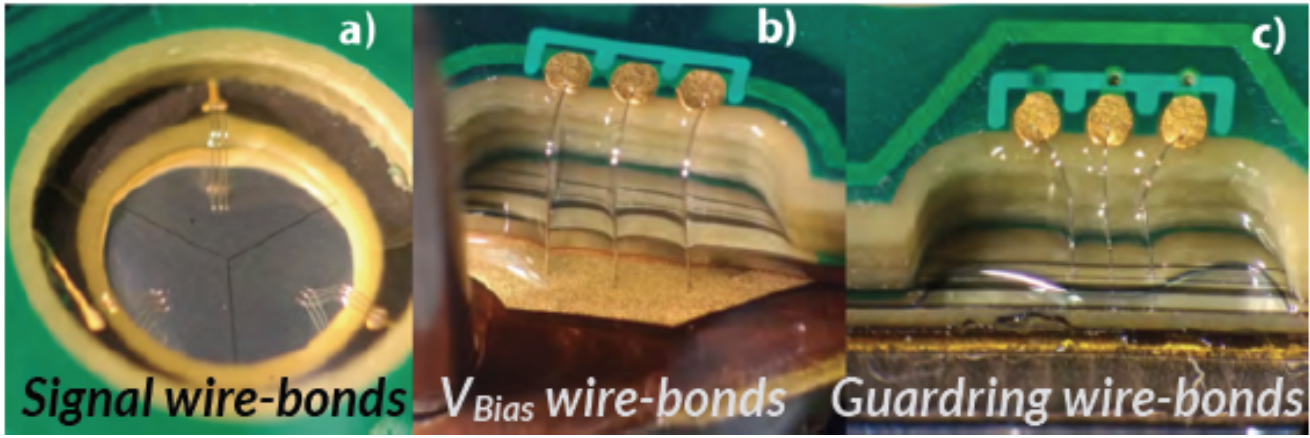
HGCAL Modules





8 inch HGCAL Silicon module assembly set-up
(At one of the 6 module assembly centers worldwide)

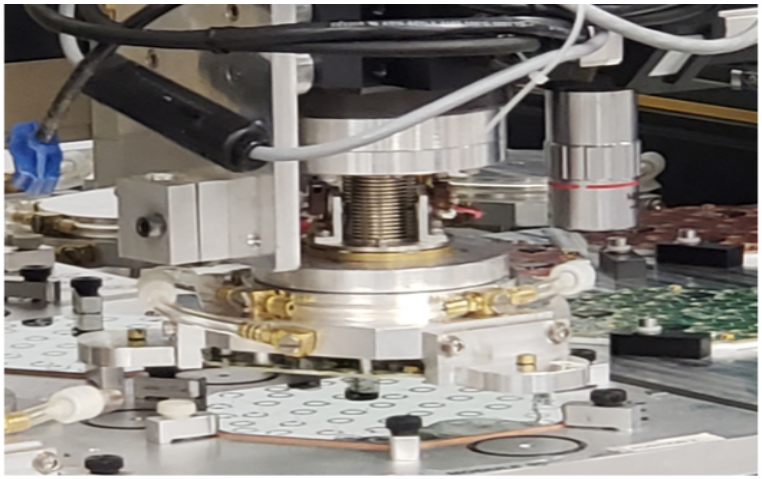


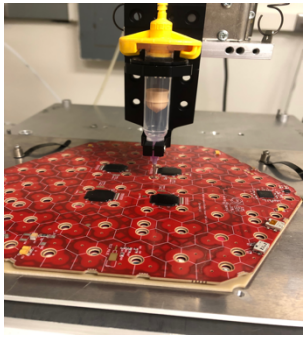


New: 8” Module Assembly

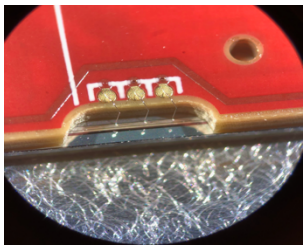
- **Five 8” Modules** built at UCSB pilot Module Assembly Centre (MAC) in June/ July

- Four modules shipped to CERN in August for extensive testing
  - All modules functional





- Gantry head tools for 8” modules have since been fabricated and tested at UCSB ready to be sent to the other MACs



Taiwan MAC

- Facility commissioned in March 2019
- In April we assembled a full module.
- On-going R&D in tooling, bonding, encapsulating, biasing.

Milestone: completed a 3-year setup/commissioning phase

Scintillators, SiPMs, Tileboards

Scintillators and SiPMs

In process of deciding on tile production techniques then materials

Candidates:

- Cast and molded individual tiles
- Cast macro-tile arrays

Criteria: Performance, cost, practicality

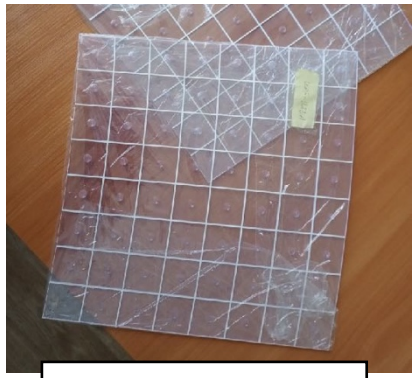
- Individual tiles and arrays have a different assembly and QC sequence

Recent Progress:

Beam tests and simulations ongoing

Radiation tolerance measurements

Individual wrapped tiles from ISMA, Kharkov



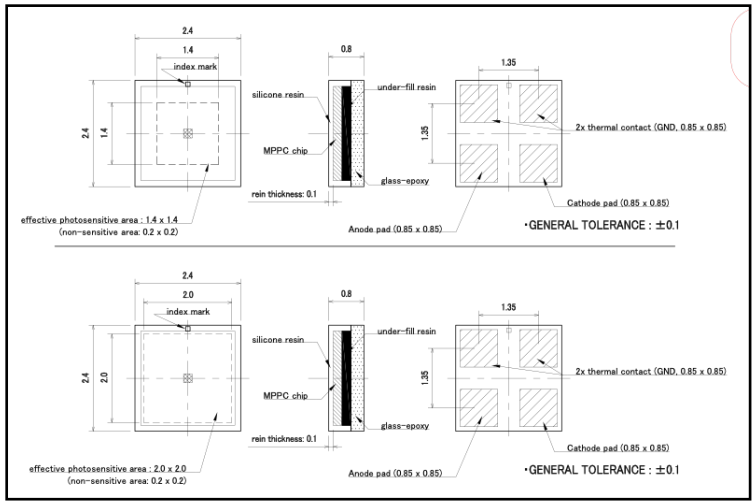
Macro-tile from ISMA, Kharkov

Prototypes in custom packaging ordered

- Good thermal conductivity
- Rad-hard window
- Common footprint for 2 and 4mm^2
- Expected in May 2020
- Plan to make irradiation studies, mount on tileboards, continuing test until end-2020

SiPMs for first tileboard prototype already in-hand

- Ordered earlier
- Same micro-structure but standard surface mount package



Scintillator-Tileboard prototype

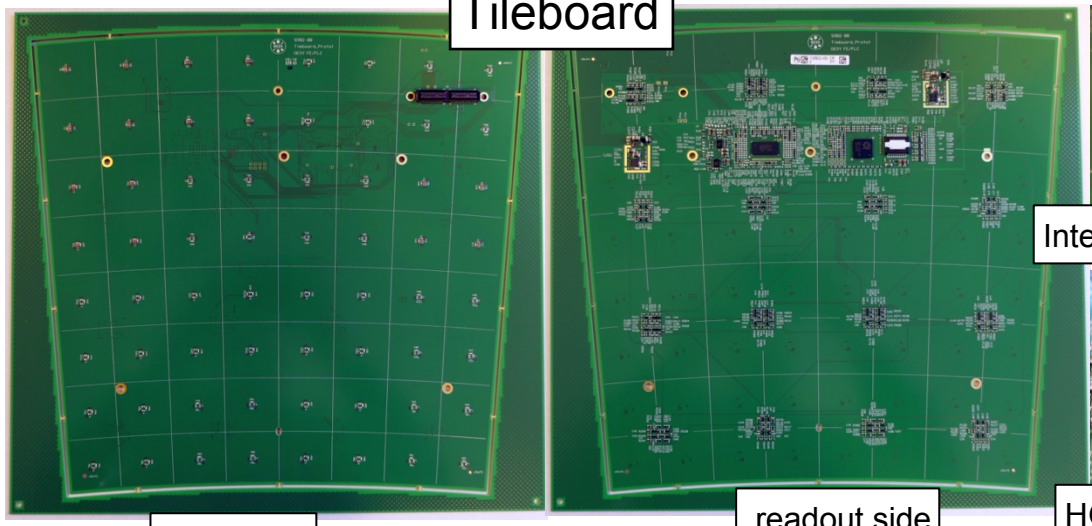
Prototype TB-1 produced

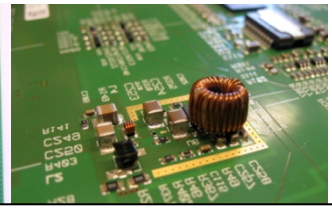
The prototype hosts:

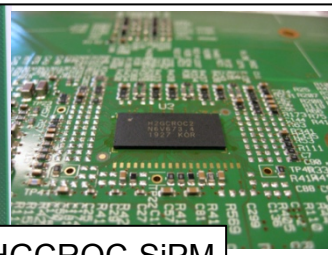
- SiPMs
- HGCROC-V2-SiPM
- GBT-SCA (slow control)
- FEAST (DCDC)
- LED system

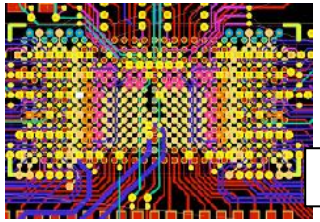
Test environment is ready

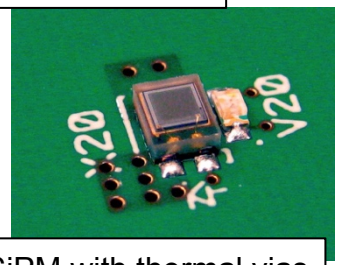
- Starting with FPGA evaluation board (KCU105)
- Test procedures implemented, based on those used for Si HGCROC-V2
- Twinax adapters in production, PCBs produced

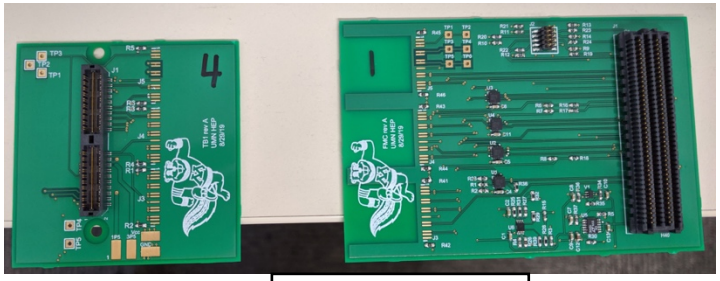


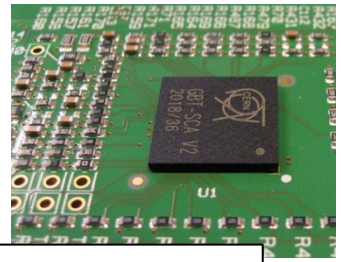

Integrated DCDC converter


HGCROC-SiPM


Detail of layout


SiPM with thermal vias


Twinax adapters


GBT-SCA (control)

Engineering

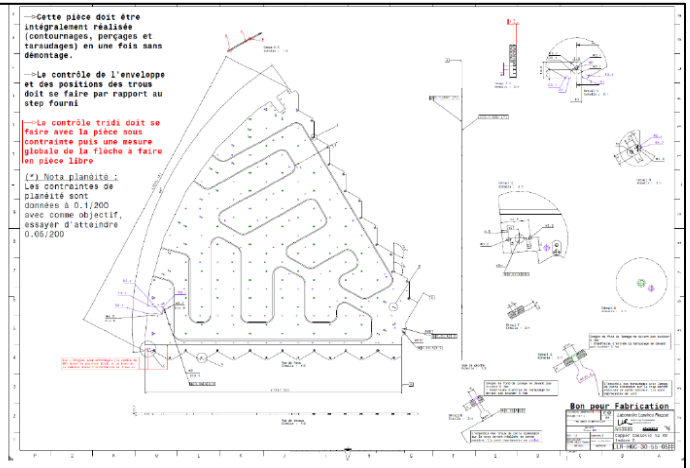
CE-E Cassetes

Led by LLR-CERN

First CE-E copper plates production feedbacks

- Thickness tolerance : 6mm +/-0.1mm
- Flatness tolerance : 0.1mm/200mm or better
- Locating precision : 0.05mm
- Contour tolerance : +/-0.05mm
  - Taking a CTE of 17.7 x 10^{-6} a tolerance of +/-0.05mm could be reached with a thermal control the room of +/-2°C or worse.

Industrially-produced CE-E Cassette cooling plate prototypes



Picture of the 2 cassettes received at LLR during summer

1500 mm

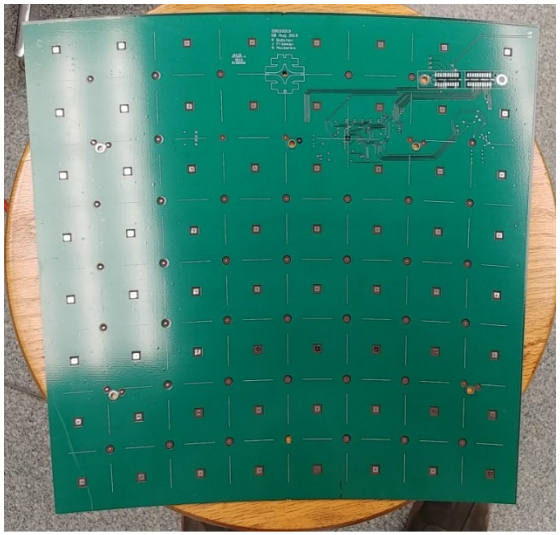
3000 mm

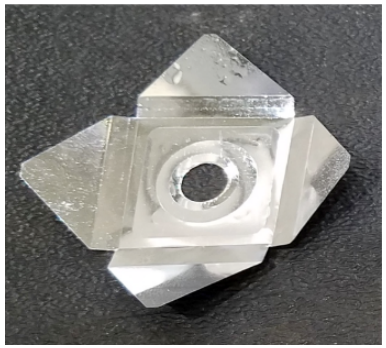
CE-H mixed Si/Scintillator Cassettes

Mixed Cassette Mockup: Thermal and mechanical tests of the mixed silicon/scintillator cassette design

FNAL-FSU-NIU

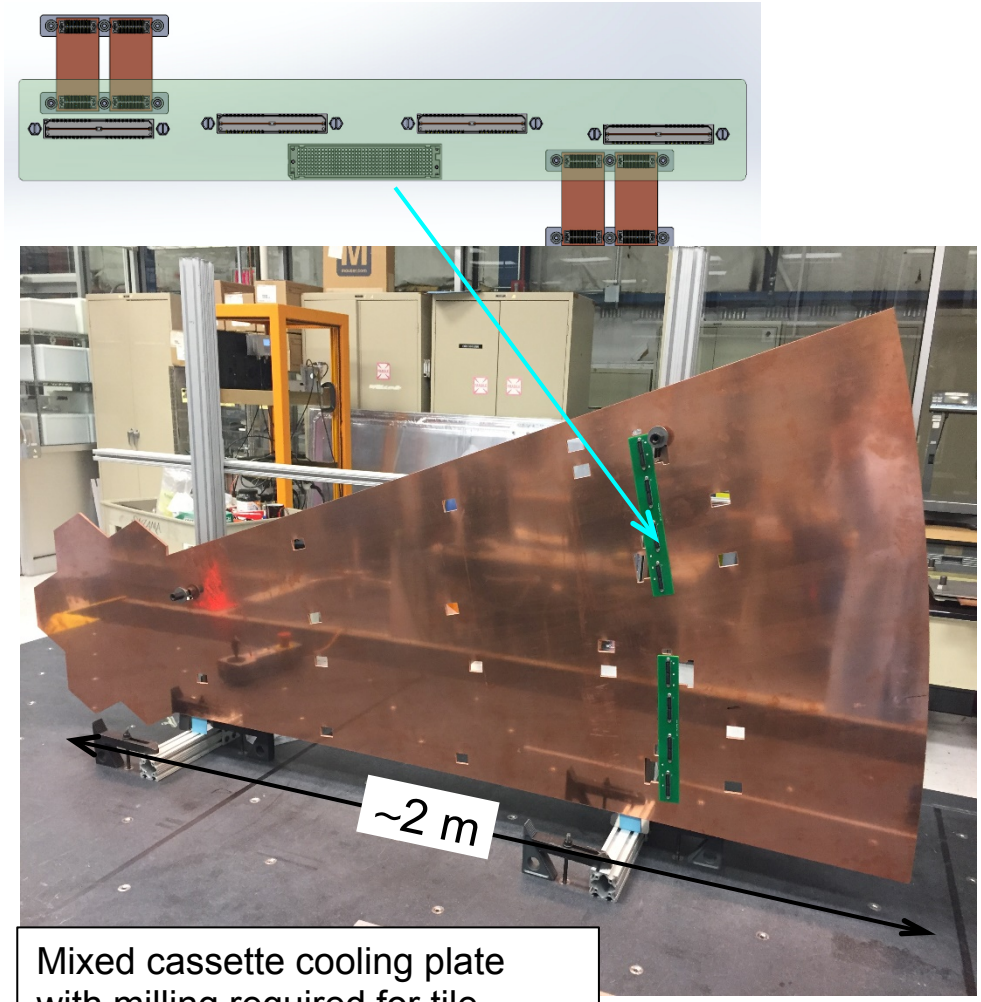
Mockup SiPM-on-tile PCBs with connectors and RTDs





Production and wrapping of tiles for mockup cassette

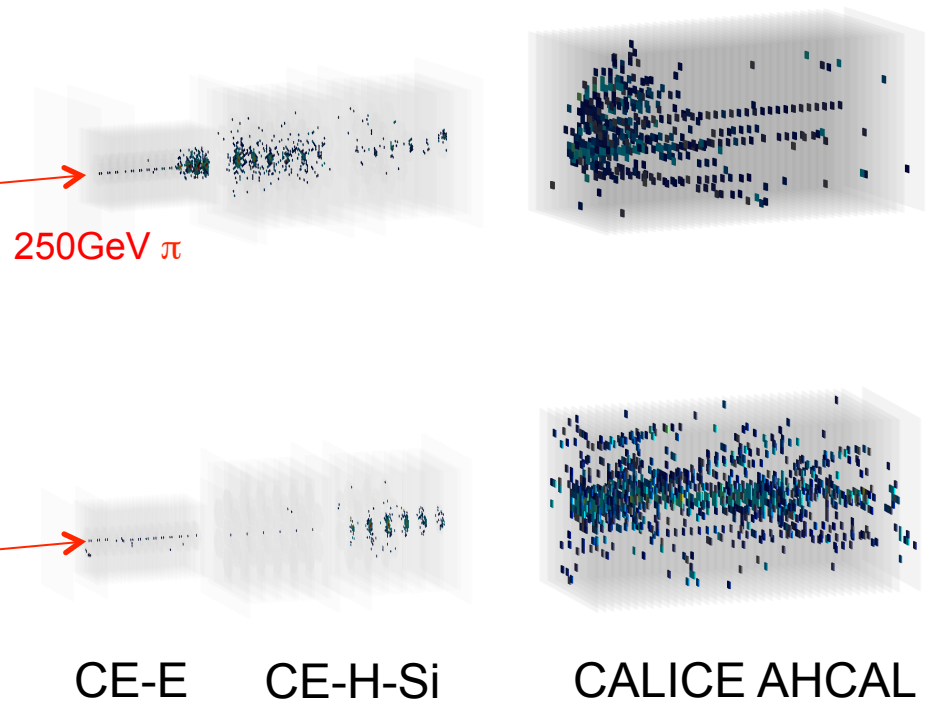
Mockup wing board PCBs (part of motherboard assembly) in production

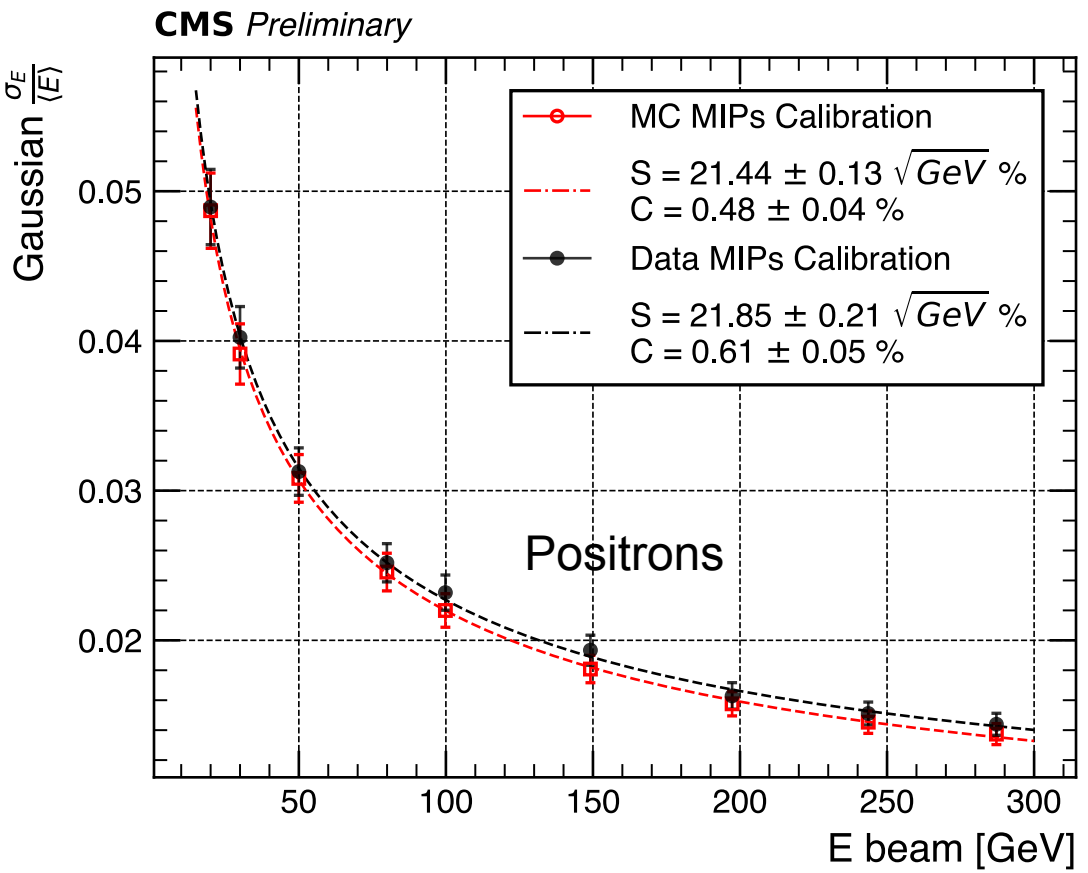


Mixed cassette cooling plate with milling required for tile module PCB electronics

Beam Tests

2018 Beam-test results





6 publication drafts are close to submission

Recent progress Summary (I)

Silicon Sensors

8” Frame contract placed, technical issues identified with 8” process and followed up with HPK, next iteration of LD and HD prototypes ready

Silicon Modules

First 8” prototypes made and tested, 8” tooling developed, MAC preparations advancing

SiPM/Scintillator system

Deep evaluation of the SiPMs scintillator choice, automation of wrapping and tileboard assembly advancing, tileboard v1 produced

Electronics

HGCROC: v1 radiation damage issues diagnosed, v2 received, packaged, and under test, v3 design advancing

ECON: design advancing following consolidation of spec and architecture, algorithms chosen

Hexaboards: LD and HD 8” prototypes designed for V2 ROC

Tileboards: V1 prototype in hand (for ROC V2)

Front-end integration studied in detail, motherboard ‘engine’ prototype made

Timing distribution: clock quality measured along a realistic path

Prototype backend boards received, first daughter cards under test, firmware schematics developed

Recent progress Summary (II)

Cassettes

Full scale cooling plate prototypes made for CE-E, options, CE-H mixed mockup activity begun

Mechanical Engineering

Extensive engineering studies of CE-H mechanics, including support cylinder, absorbers, fixations

CE-E support cylinder prototyped and load-test prepared

CE-E mechanical pieces prototyped

Services integration being modeled in detail, transfer line integration design well advanced

System and Beam tests

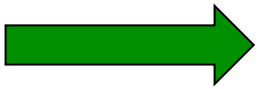
2018 test beam analysis essentially complete, several publications drafted

DPG

Geometry and simulation of front-end response improved, reco algorithms advancing

QA/QC

EDMS extensively used for reference documentation and interface control, production database development (together with Tracker) advancing well



Overall excellent progress in all respects, however still many challenges lie ahead

Extra Slides

8-inch Sensors

1) Oxide quality

8” process has higher flat band voltage => higher oxide charge density compared to 6”

- *Could be an issue* for the radiation resistance. **Being checked by inter-pad resistance measurements**
- HPK working to better reproduce 6” oxide quality on 8” line: **will study this on forthcoming prototypes**

Parameter	Tracker 6“	Hgcal 8“
Flat band voltage	2.2±0.2 V	5.4±0.2 V
Oxide charge	(4.3 ± 3.4) $\times 10^{10}$ cm^{-3}	(1.2 ± 0.6) $\times 10^{11}$ cm^{-3}
Oxide thickness	705 ± 5 nm	726 ± 15 nm

2) Wafer Oxygen content

8” wafers have much lower oxygen content compared to 6” wafers

- *Could be an issue* for the radiation resistance. **Being checked in the radiation testing program (charge collection efficiency, CCE)**

Oxygen concentration		'alue toms/cm3] MAX
6inch wafer	FZ P 320	6.5E17
	Epi P 50	1.5E18
	Epi P 100	1.5E18
8inch wafer	P-FZ (for 300um and 200um)	4.5E16
	P-Epi 120	1E16

8-inch Sensors

3) Backside mechanical fragility

8” sensor processing => thin backside implant (~1μm vs ~30μm for 6” sensor processing)

Mitigation:

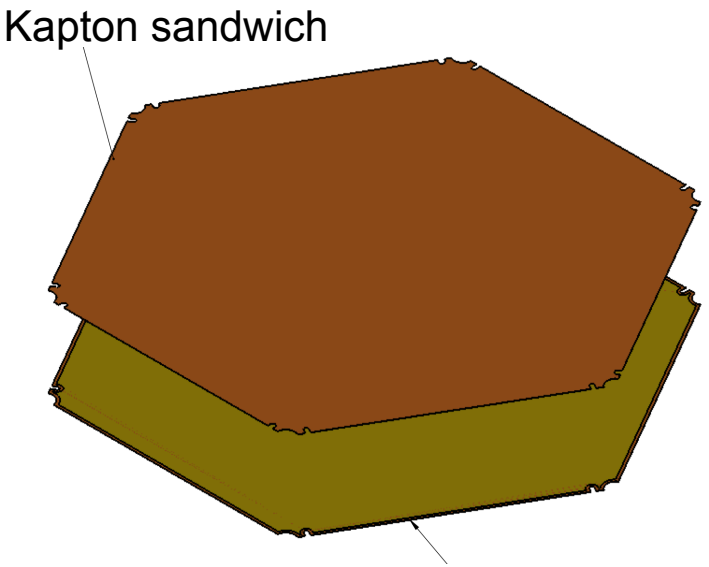
(1) **Protect sensor backside** from possible mechanical damage during handling/assembly

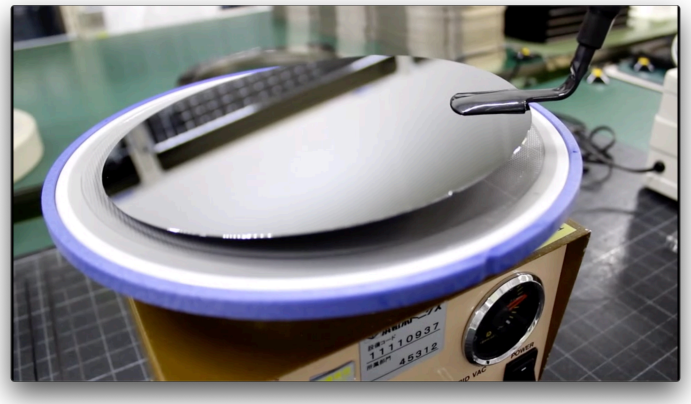
Two options under discussion with HPK

- Module includes Kapton foil to electrically decouple sensor backside from mechanics: consider applying this at HPK prior to delivery
- Deliver sensors on dicing tape/ring, remove on gantry assembly table

(2) **Avoid contacting sensor backside** with metal tools/chucks

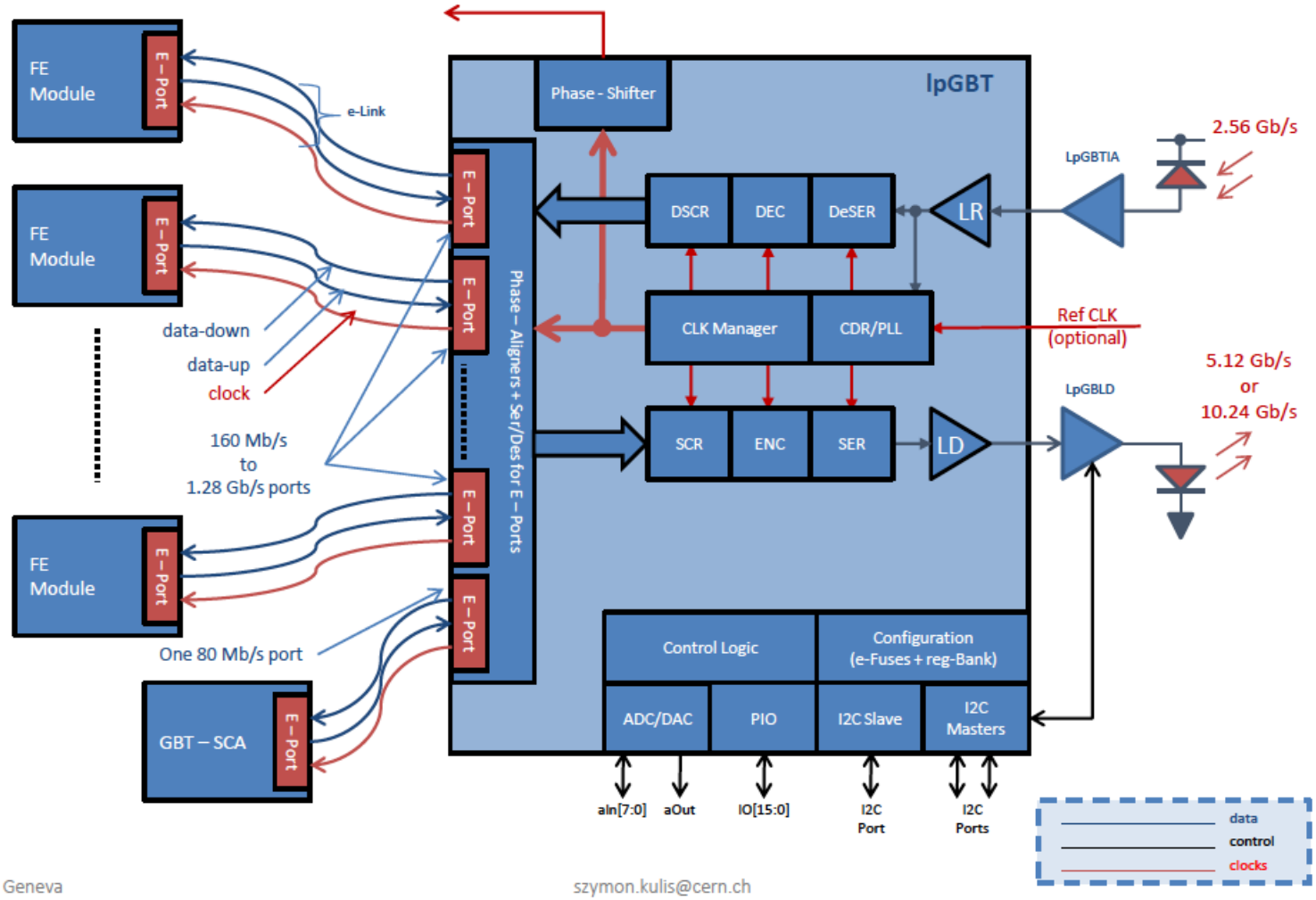
- Front side bias for testing on probe station – design changes made to the layout





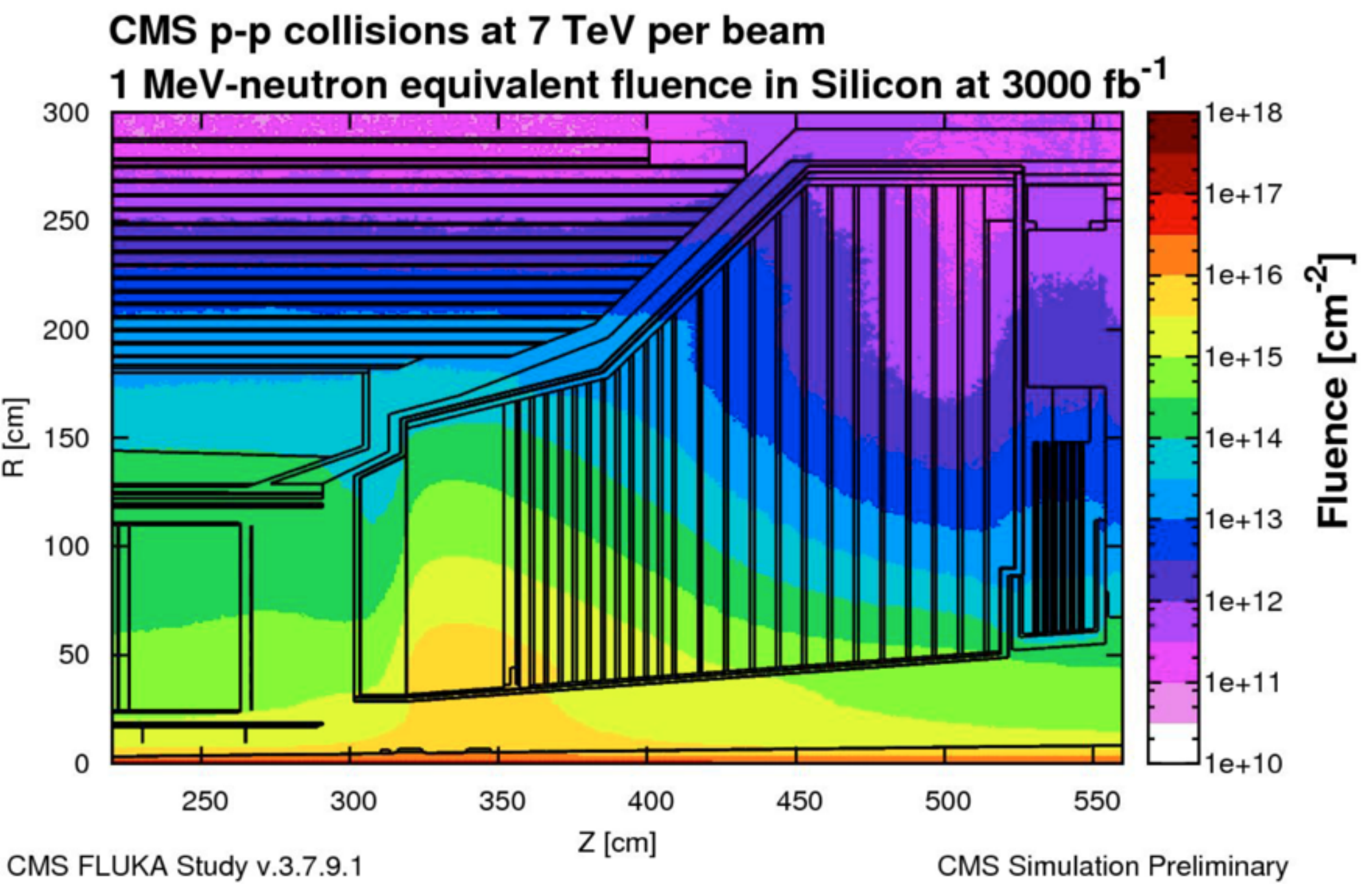
Dicing frame and foil („Nitto“ tape)

lpGBT: Block Diagram (simplified)



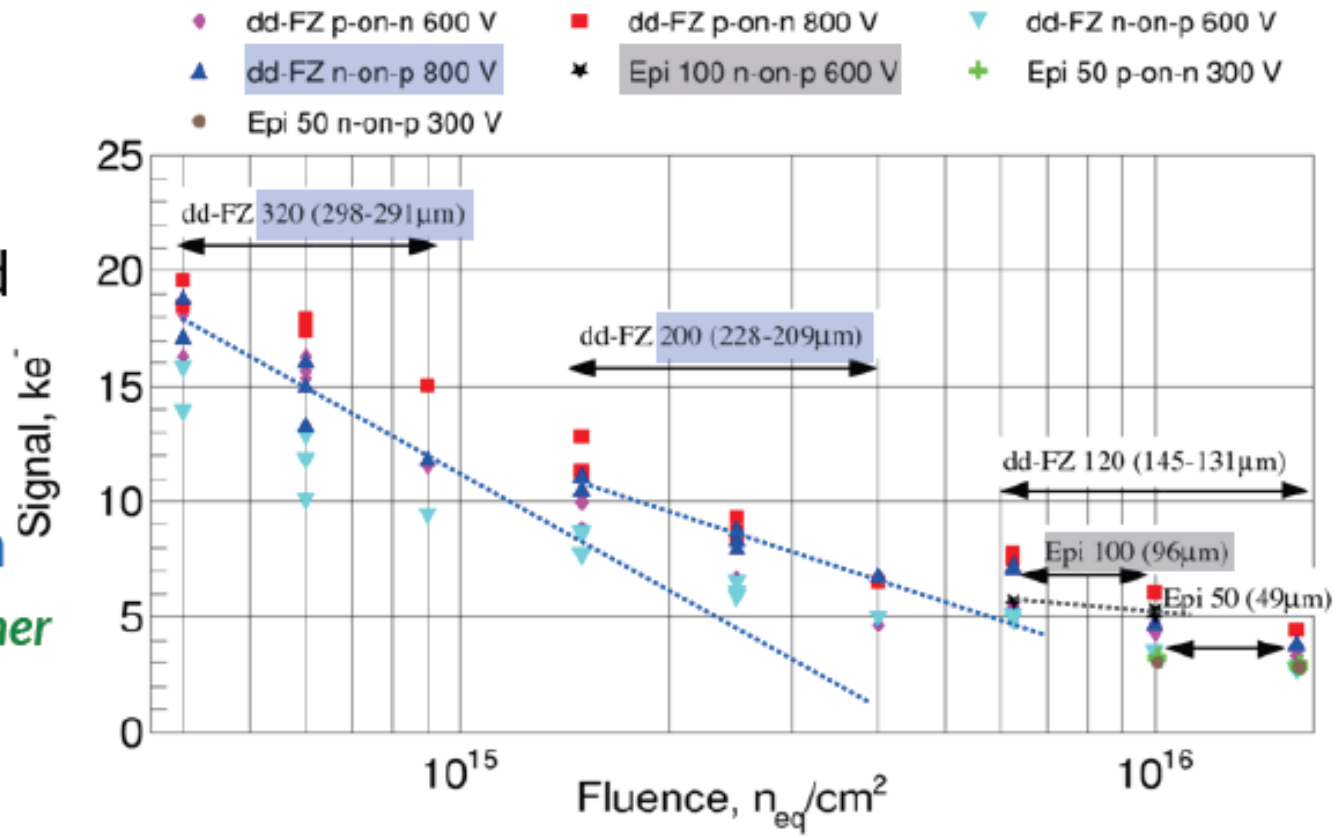
Data Tranceiver Serializer/Deserializer

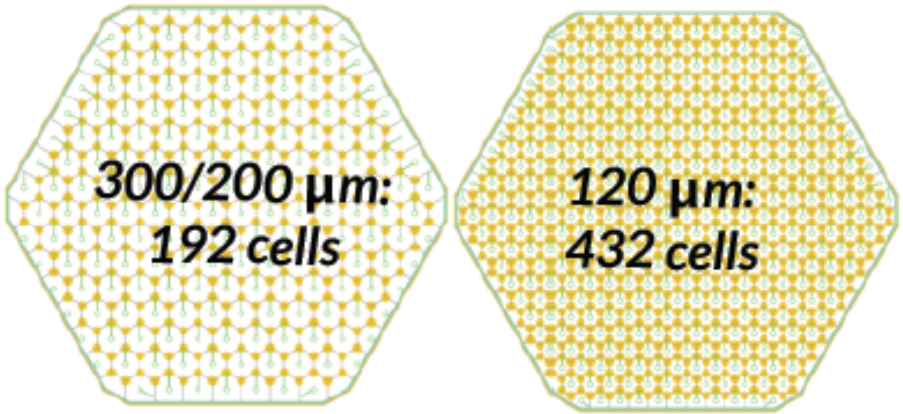
Expected radiation dosage vs R,Z



HGCAL Silicon sensors

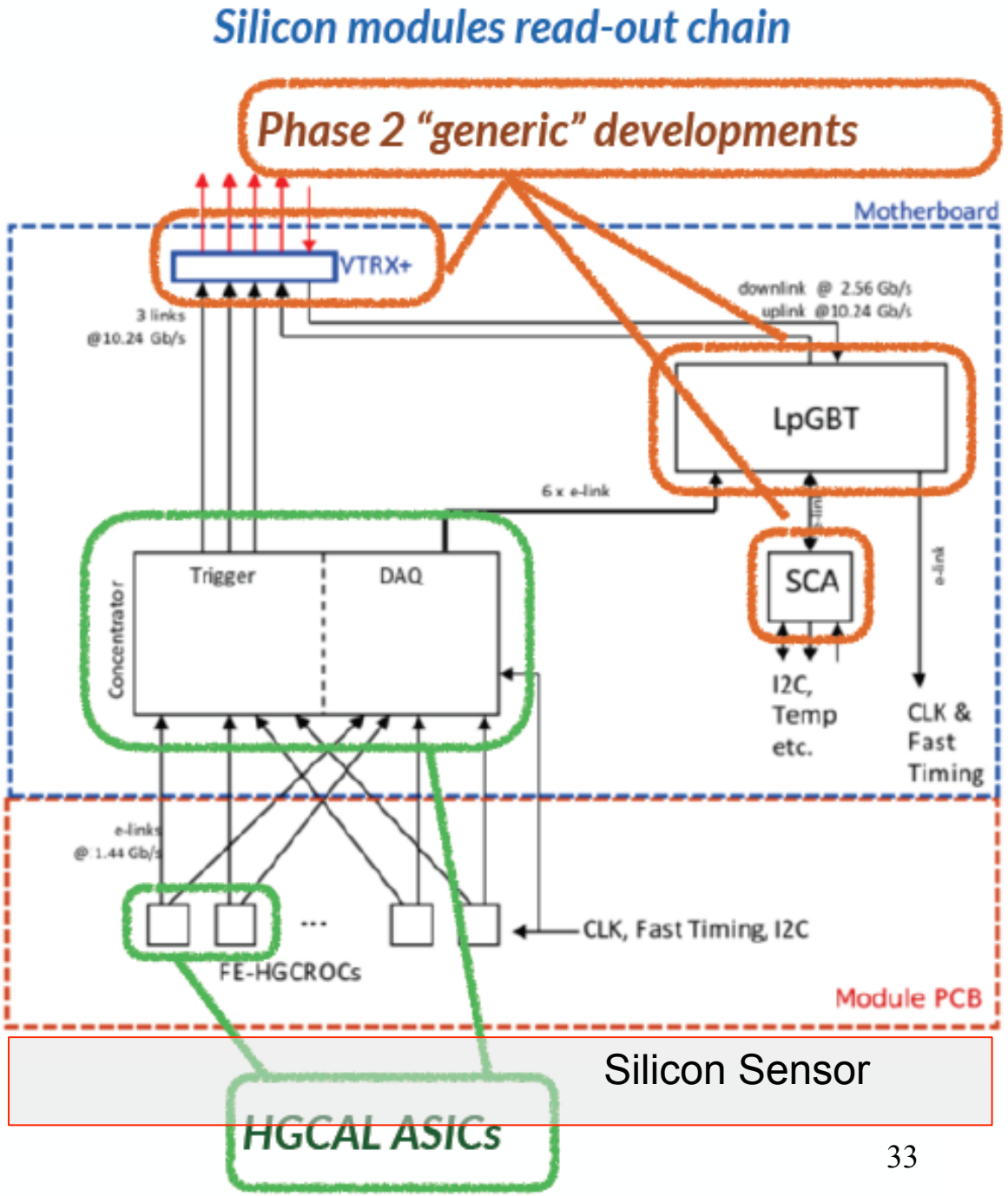
- 8 inch wafers
- Hexagonal sensor geometry
- Planar p-type DC-coupled sensor pads
- Active thickness:
  300 µm, 200 µm, 120 µm
  - ***Advantage of deploying thinner sensors in the higher fluence regions***
    - ***More tolerant to large neutron fluences***
  - ***Reduced cell size in thinner sensors***
    - ***Keeping the capacitance reasonable***



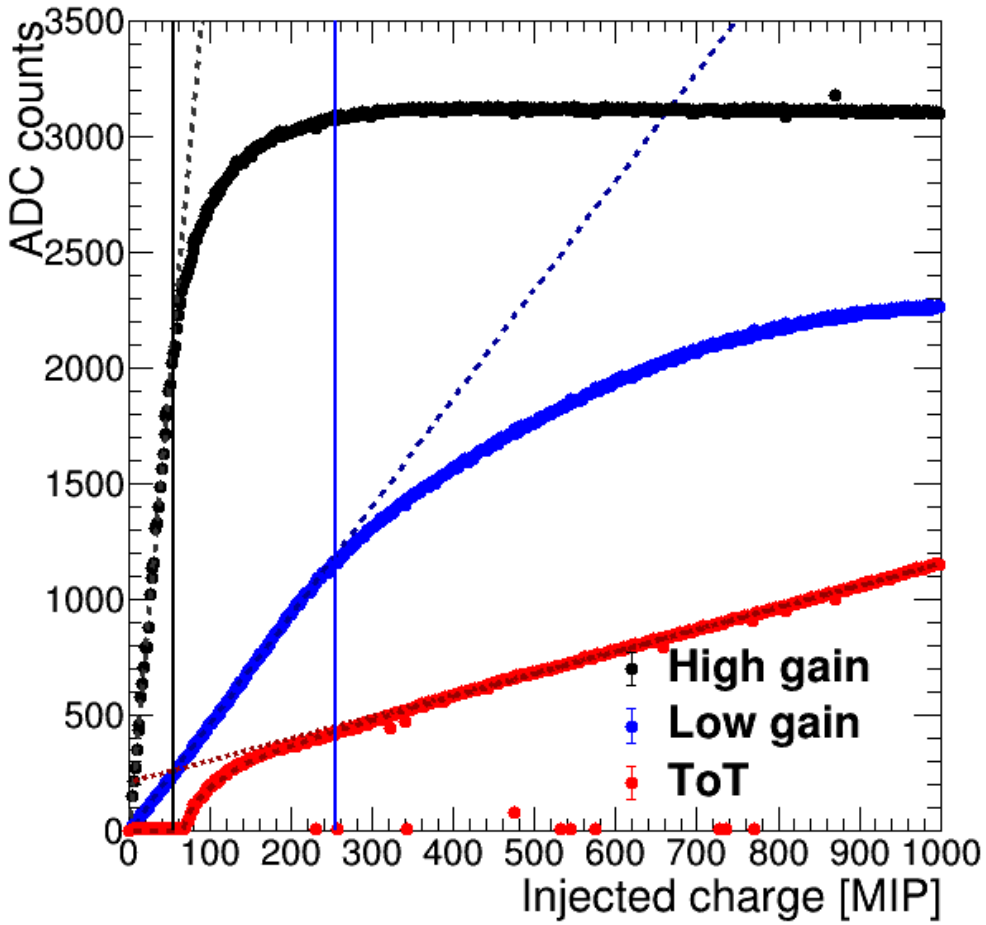


FEE Read-Out Chain

- The front-end electronics
  - Measures and digitizes the charge
    - 10bit ADC (0.2fC - 100fC)
    - 12bit TDC (50fC to 10pC)
  - Provides a high precision measurement of the time of arrival of the pulses
    - 10bit TDC with 25ps bins
  - Transmits the digitized data to the back-end electronics
- Similar front end electronics for the readout of the SiPMs



Pad energy reconstruction: LG,HG,ToT



$$A'_{HG} = \begin{cases} A^{TOT} \cdot m_{LG/TOT} \cdot m_{HG/LG} & \text{, if } A^{LG} > TP_{LG} \\ A^{LG} \cdot m_{HG/LG} & \text{, else if } A^{HG} > TP_{HG} \\ A^{HG} & \text{, otherwise} \end{cases}$$

$$E^{Si}_{pad}[MIP] = A'_{HG} \cdot M_{MIP/HG},$$