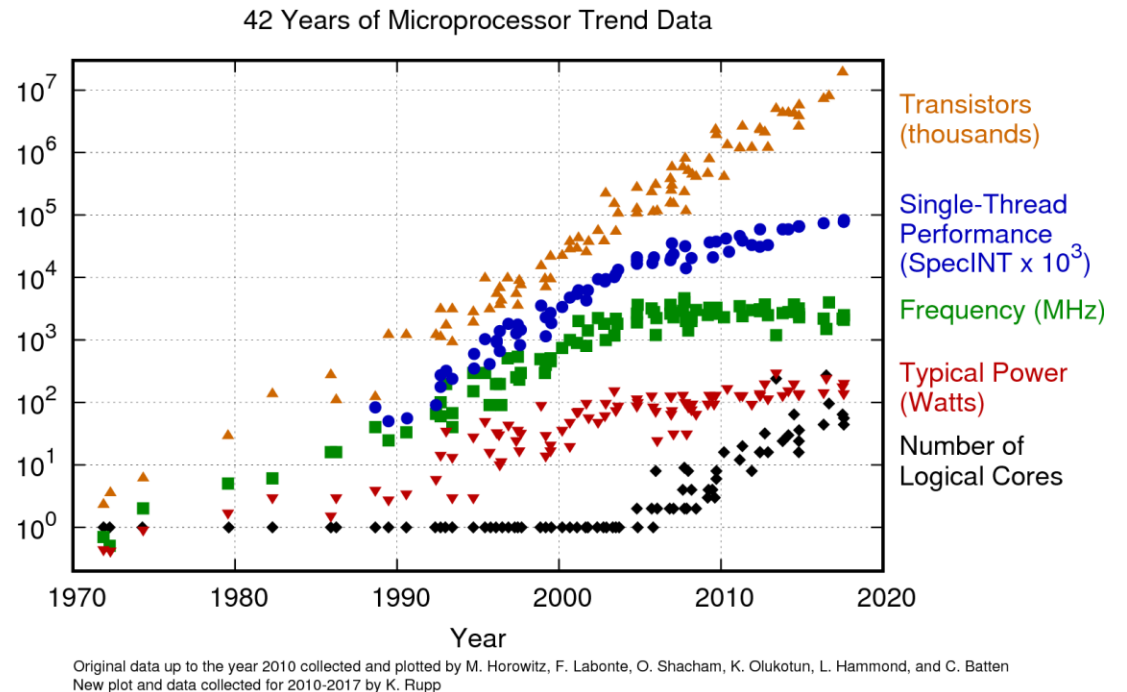# Introduction to TDAQ session

Federico Alessio (CERN), Zhen-An Liu (IHEP), Stewart Martin-Haugh (RAL)

Horizon scanning for TDAQ technology

- CPU performance has flatlined (although increase in number of cores)

- Increasing exploitation of FPGAs, GPUs by industry and HEP

- Co-processor support needs to be part of CEPC software design

42 Years of Microprocessor Trend Data

Transistors (thousands)

Single-Thread Performance (SpecINT x 10^3)

Frequency (MHz)

Typical Power (Watts)

Number of Logical Cores

Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten
New plot and data collected for 2010-2017 by K. Rupp

Overview of session

- 大家好！
- What do current and near-future experiments have to offer CEPC?
- What are the trends in technology and techniques over the next few years?
- Should have plenty of time for discussion during the session
  - As long as speakers stick to time!
- 谢谢 to all speakers and participants