清華大學
Tsinghua University

核电子学实验室
Laboratory of Nuclear Electronics

Progress on Low Power FEE ASIC Development for TPC

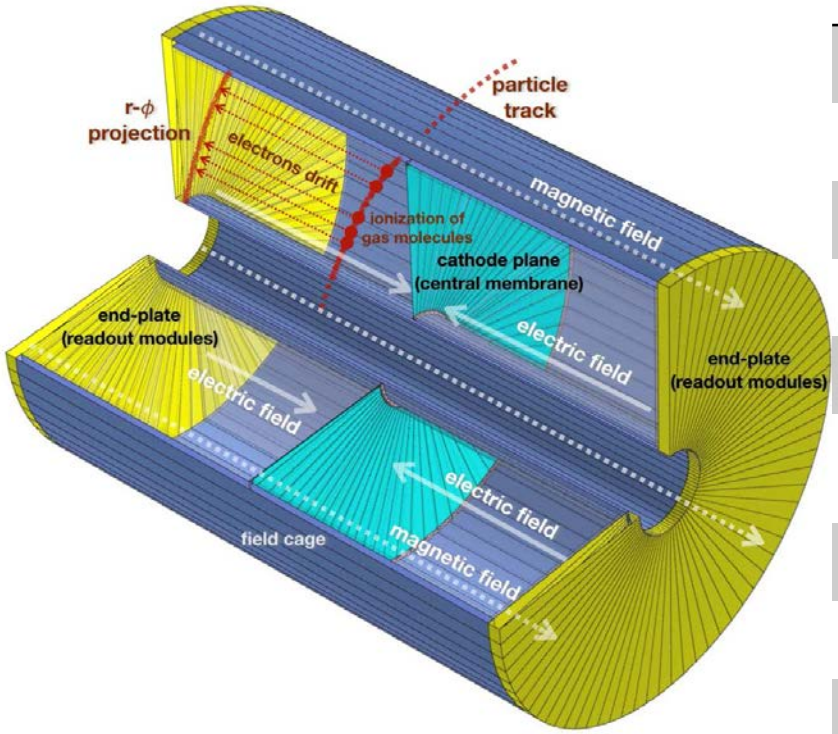
Wei Liu[1,2], Xinyuan Zhao[1,2] ,Zhi Deng[1,2], Fule Li[3], Xian Gu[3], Yulan Li[1,2], Huirong Qi[4]

[1] Department of Engineering Physics, Tsinghua University, Beijing, China
[2]Key Laboratory of Particle & Radiation Imaging, Ministry of Education, Beijing, China
[3]Institute of Microelectronics, Tsinghua University, Beijing, China
[4]Institute of High Energy Physics, Chinese Academy of Science, Beijing, China

Outline

- Introduction
- Progress on ASIC Design
- Progress on Digital Filters and Data Compression
- Summary & Future Plan

Introduction



Momentum resolution (B=3.5T)	$\boldsymbol{\delta(^1/_{p_t} \approx 10^{-4}/GeV/c)}$
δ_{point} in $r\Phi$	<100 μm
δ_{point} in rz	0.4-1.4 mm
Inner radius	329 mm
Outer radius	1800 mm
Drift length	2350 mm
TPC material budget	$\approx 0.05X_0$ incl. field cage $< 0.25X_0$ for readout endcap
Pad pitch/no. padrows	$\approx$ 1 mm $\times$ (4~10mm) /$\approx$ 200
2-hit resolution	$\approx$ 2 mm
Efficiency	>97% for TPC only ($p_t > 1GeV$) >99% all tracking ($p_t > 1GeV$)

- TPC can provide large-volume high-precision 3D track measurement with stringent material budget
- In order to achieve high spatial resolution, small pads (e.g. 1 mm x 6mm) are needed, resulting ~1 million channel of readout electronics
- Need low power consumption readout electronics working at continuous mode

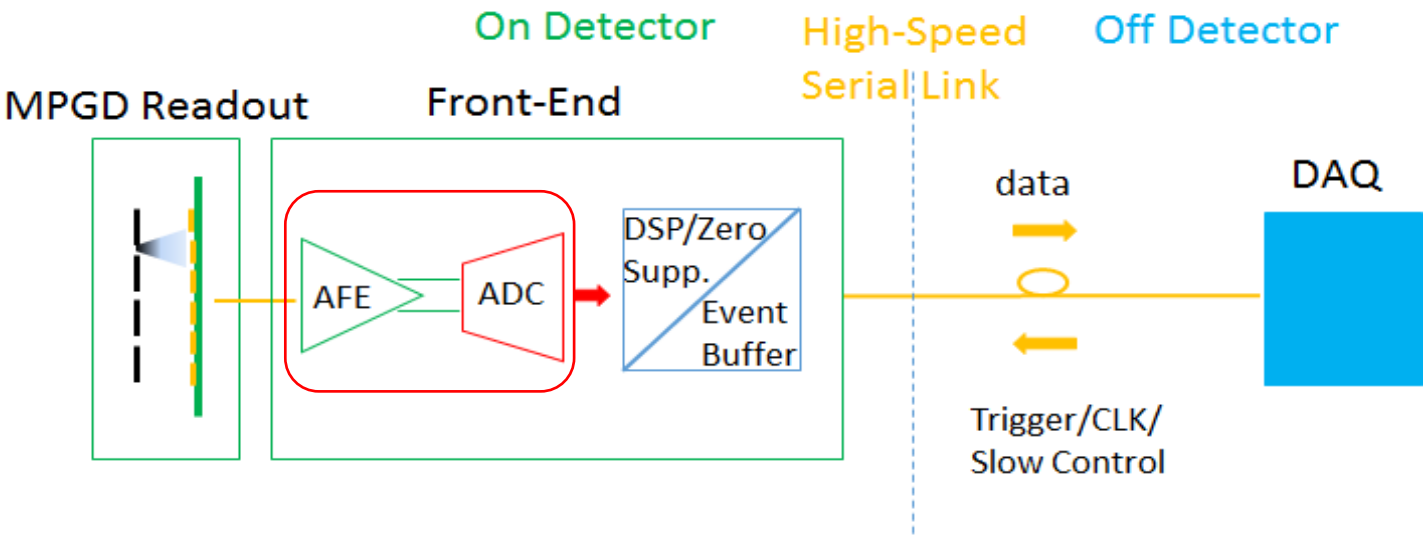
Current TPC Readout ASICs

	PASA/ALTRO	AGET	Super-ALTRO	SAMPA
TPC	ALICE	T2K	ILC	ALICE upgrade
Pad size	4x7.5 mm^2	6.9x9.7 mm^2	1x6 mm^2	4x7.5 mm^2
Pad channels	5.7 x 10^5	1.25 x 10^5	1-2 x 10^6	5.7 x 10^5
Readout Chamber	MWPC	MicroMegas	GEM/MicroMegas	GEM
Gain	12 mV/fC	0.2-17 mV/fC	12-27 mV/fC	20/30 mV/fC
Shaper	CR-$(RC)^4$	CR-$(RC)^2$	CR-$(RC)^4$	CR-$(RC)^4$
Peaking time	200 ns	50 ns-1us	30-120 ns	80/160 ns
ENC	385 e	850 e @ 200ns	520 e	482 e @ 180ns
Waveform Sampler	ADC	SCA	ADC	ADC
Sampling frequency	10 MSPS	1-100 MSPS	40 MSPS	20 MSPS
Dynamic range	10 bit	12 bit(external)	10 bit	10 bit
Power consumption	32 mW/ch	10.0 mW/ch	47.3 mW/ch	8 mW/ch
CMOS Process	250 nm	350 nm	130 nm	130 nm

No current chips can meet the readout requirement for the CEPC TPC

- More advanced 65nm process
- Adopt simplified circuit structure such as SAR-ADC,CR-RC shaper

Architecture and Specifications of FEE



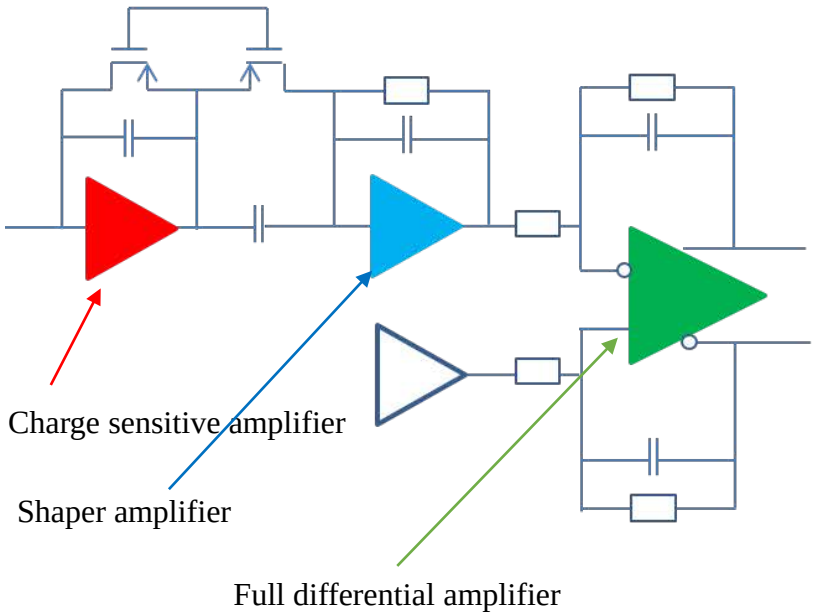
AFE(Analog Front-End)	
Signal Polarity	Negative
Detector Capacitance	5-20 pF
Shaper	CR-RC
Shaping Time	160 ns
ENC (Equivalent Noise Charge)	<500 e @ 10pF
Dynamic Range	120 fC
Gain	10 mV/fC
INL (Integrated Non-Linearity)	<1%
Crosstalk	<1%
Power Consumption (AFE)	<2.5 mW/ch

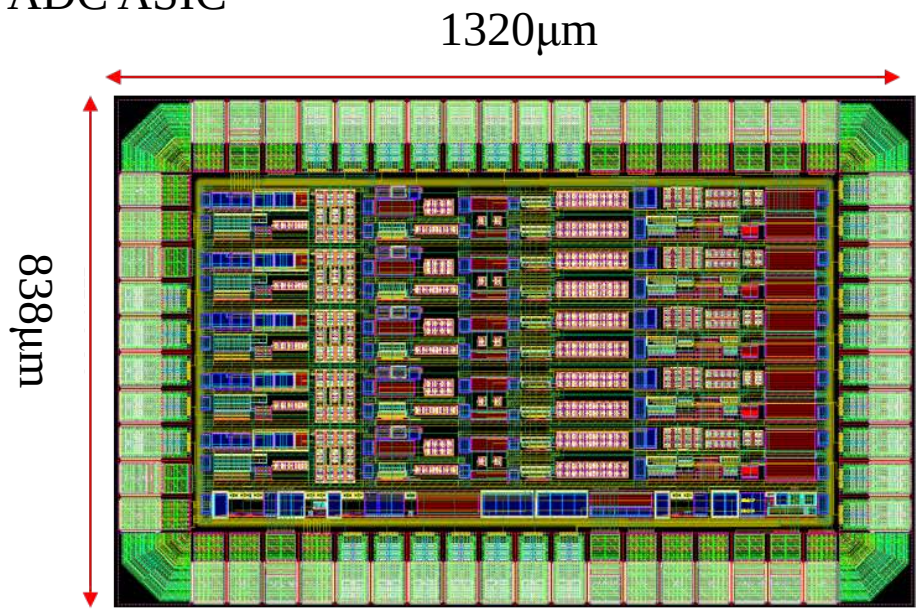
SAR-ADC	
Input Range	-0.6 V ~ 0.6 V diff.
Resolution	10 bit
Sampling Rate	40 MS/s
DNL	<0.6 LSB
INL	<0.6 LSB
SFDR @ 2MHz, 40MSPS	68 dBc
SINAD	57 dB
ENOB	>9.2 bit @ 2MHz
Power Consumption (ADC)	<2.5 mW/ch

Current Status : Analog Front-End ASIC

Three prototype chips have been taped out and evaluated during 2017→ 2018

- 5 channel Analog Front-End ASIC
- Single channel SAR-ADC ASIC
- Single channel Analog Front-End +SAR-ADC ASIC





The test results of main specifications of 5 channel Analog Front-End ASIC：

- Power consumption： 2.02 mW/channel
- Gain： 9.8 mV/fC
- ENC(equivalent noise charge)： 589 e @10pF

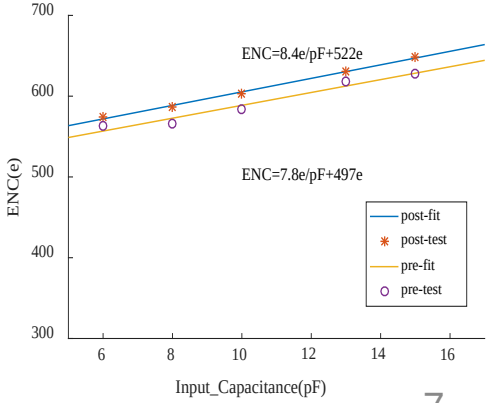
Current Status :TID Tests for Analog Front-End

Test setup:

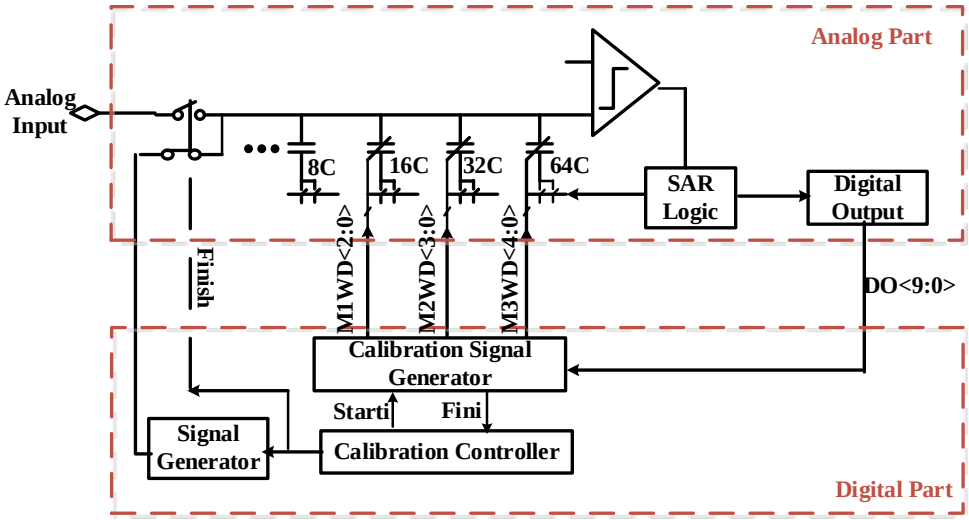
- Radiation Source: Co-60
- Does rate: 50 rad(Si)/s
- TID(total ionizing dose): 1 Mrad (Si)
- Sample no.: 3
- Chip working condition: 1.2 V supply voltage with 25 uA mater bias current

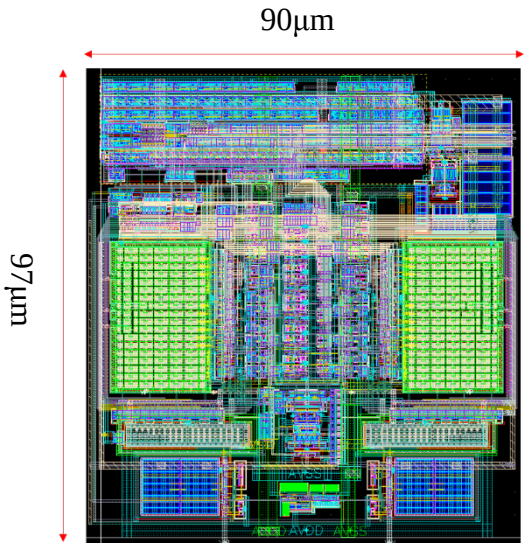
TID test results:

- The power consumption remained basically unchanged before and after TID test.
- The gain increased slightly （9.8 mV/fC→10.4 mV/fC）and the maximum integral non-linearity of there chips remained basically unchanged.
- The ENC increased slightly（589 e→605 e @ 10pF）before and after TID test.

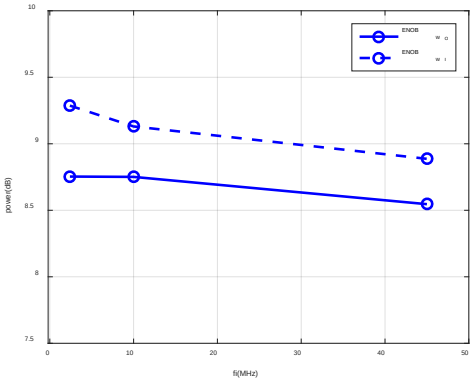


Current Status : SAR ADC





Module Name	Power(mW)
Chip	4.0
Referred Buffer Module	0.25
SAR ADC Core Module	1.0
Clock Generation Module , etc	2.75



The test results of main specifications of single SAR ADC

- The core power consumption of SAR ADC:1 mW
- Maximum INL(integral non-linearity),DNL(differential nonlinearity)=0.6 LSB
- ENOB=9.15 bit under 50 MS/s sampling rate with 2.4 MHz differential sinewave input

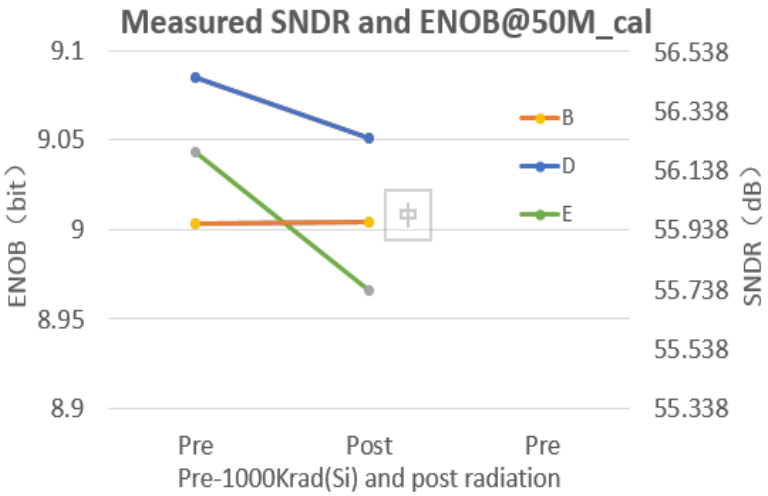
Current Status : TID Tests for SAR ADC

Test setup:

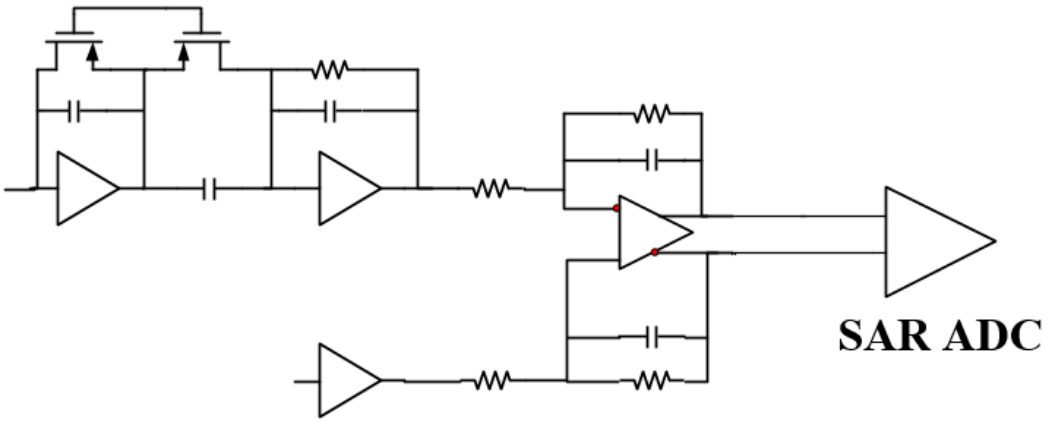
- Radiation Source: Co-60
- Does rate: 50 rad(Si)/s
- TID: 1Mrad (Si)
- Sample no.: 3
- Chip working condition: CLK=50 M, fed with 2.4 MHz sine input signal

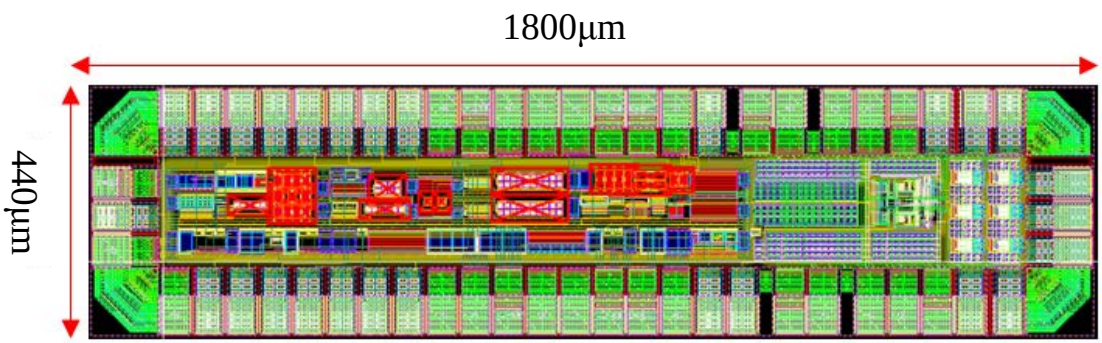
TID test results:

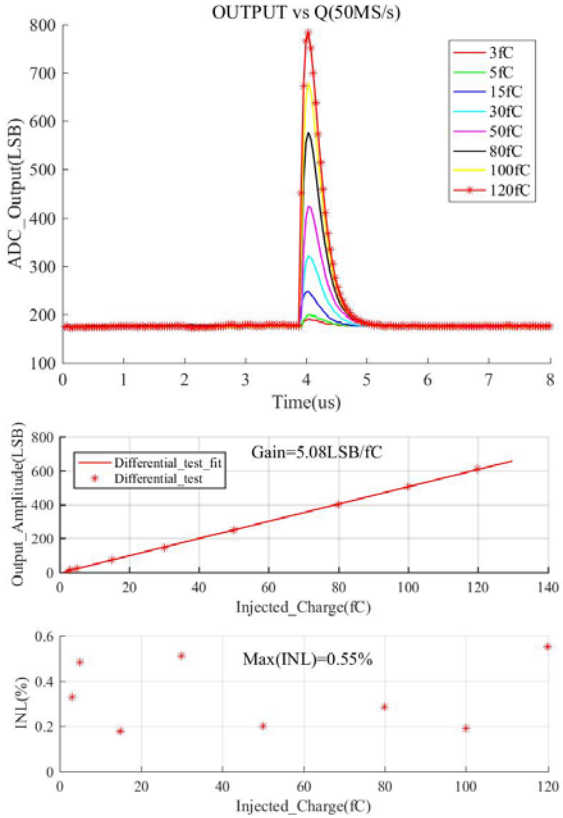
- The ENOB decreased slightly before and after TID test.
- The INL and DNL remained basically unchanged before and after TID test.



Current Status : Analog Front-End + SAR ADC



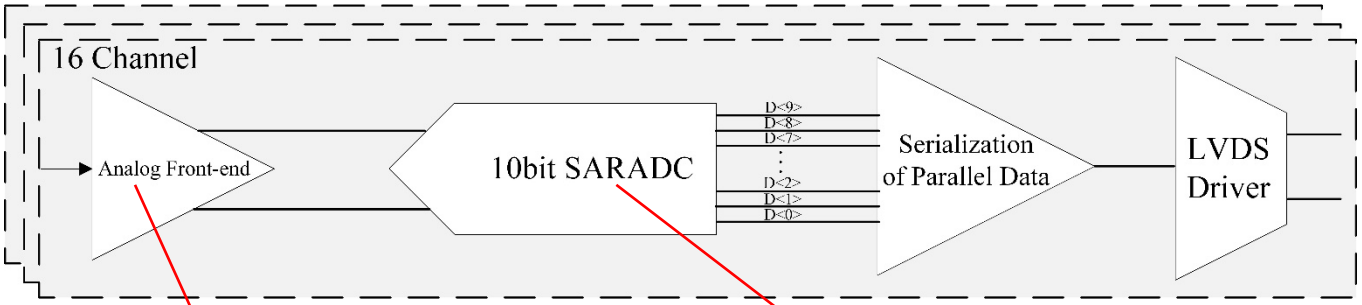


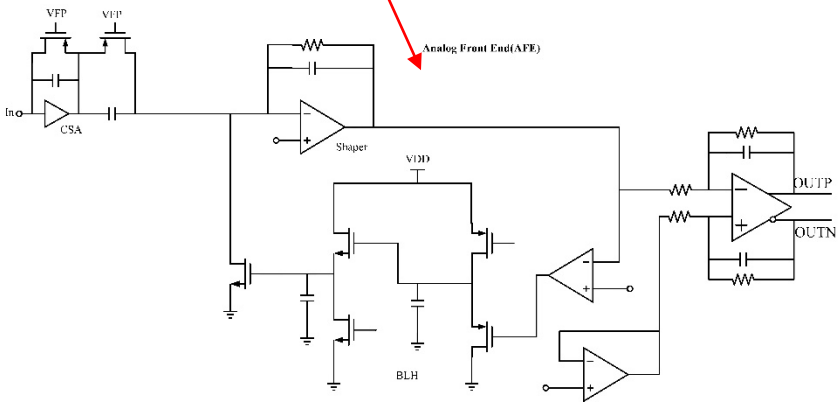


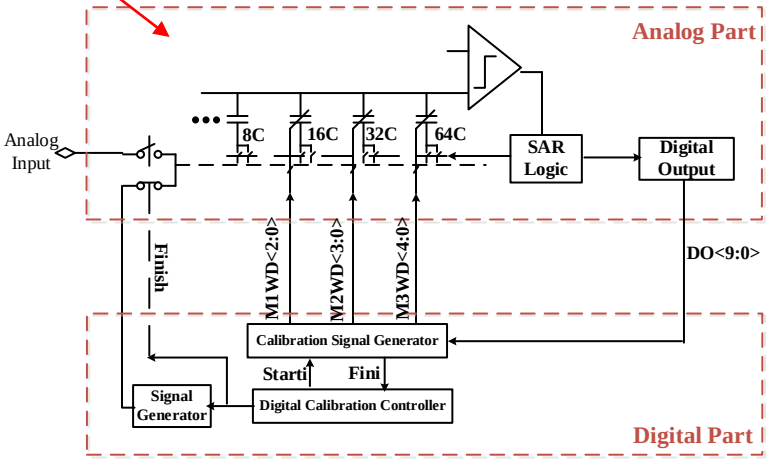
The test results of main specifications of single Analog Front-End + SARADC

- Power consumption： 2.5 mW
- gain： 5.08 LSB/fC
- ENC： 900 e @10pF

The 16-ch TPC Readout ASIC



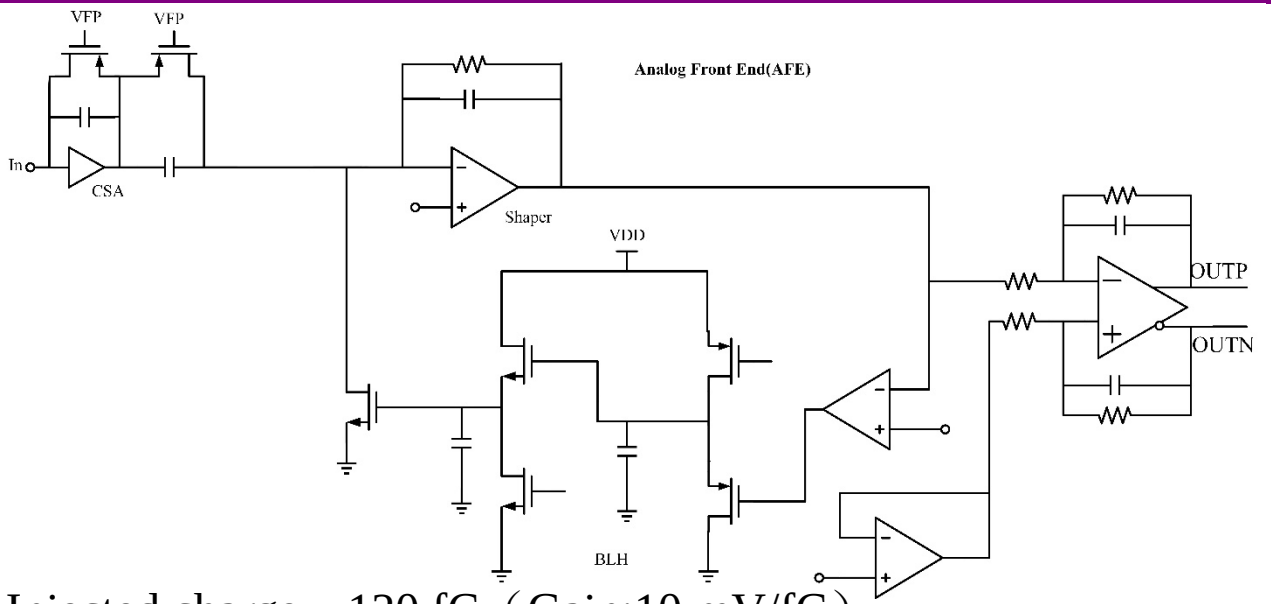




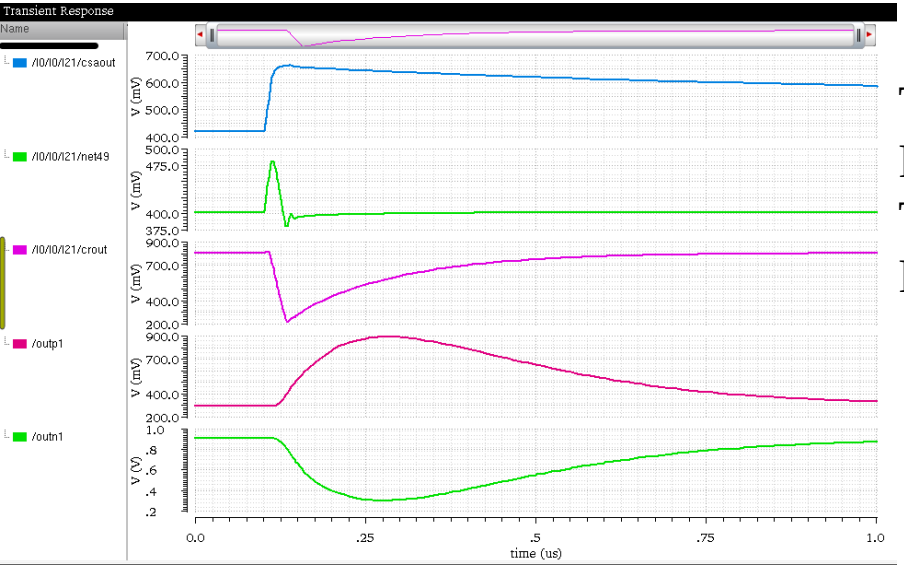
Design highlights：

- 16 channel
- Power consumption of Analog Front-end : from 2.02 mW/channel to 1.4 mW/channel
- ENC : from 589 e to 303 e @10 pF

Transient Simulation of Analog Front-End



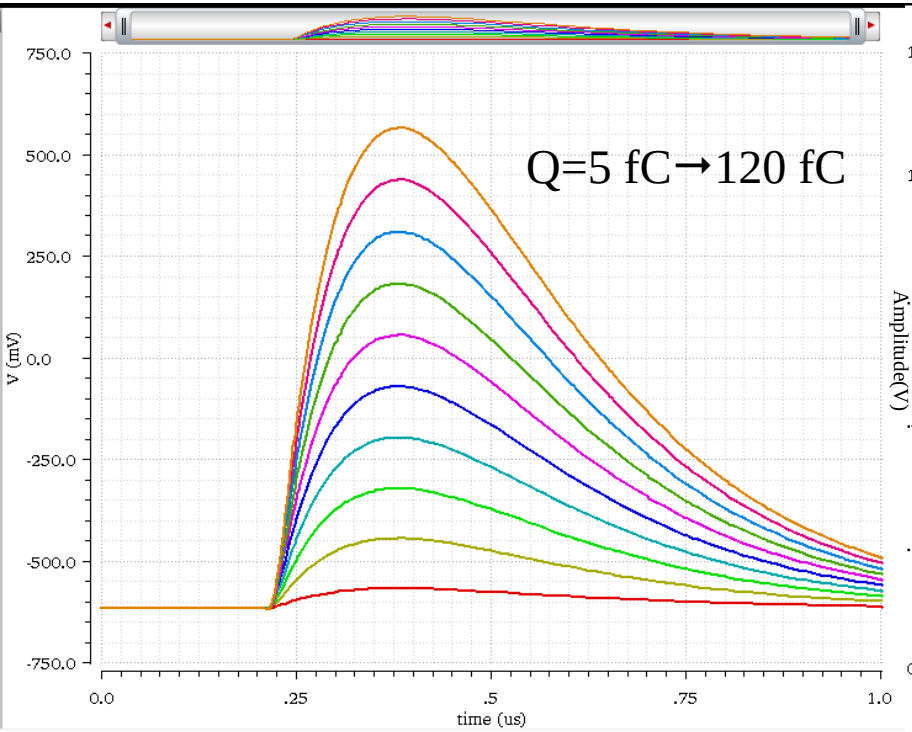
Injected charge：120 fC（Gain:10 mV/fC）

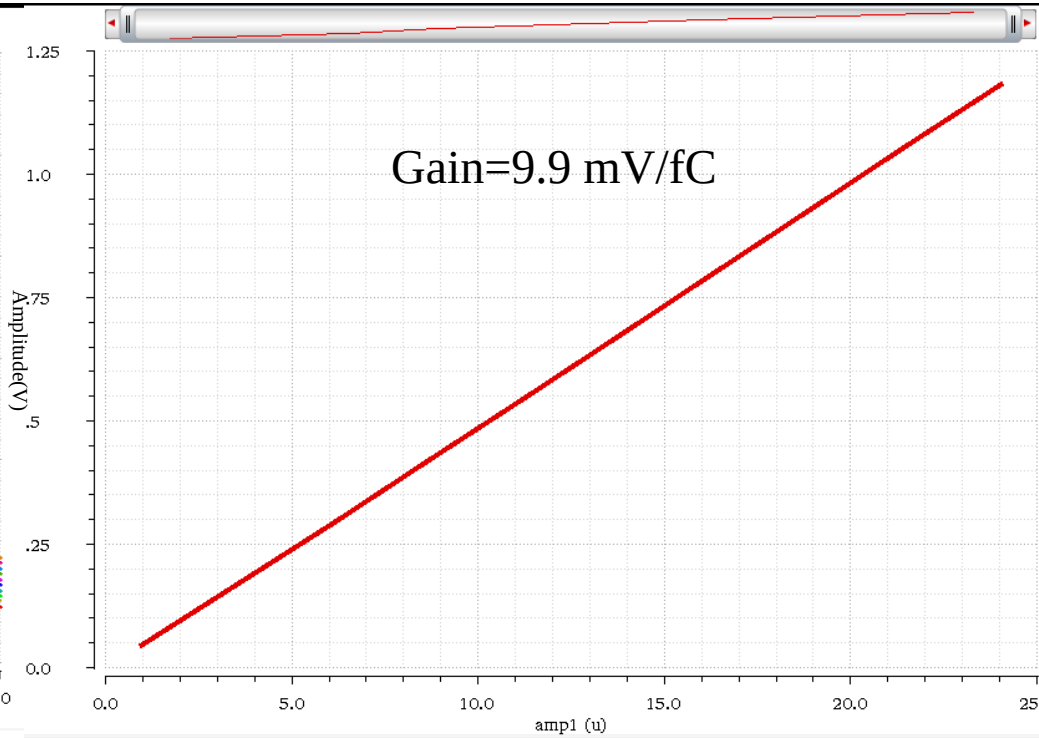


The simulation power consumption of Analog Front-end：**1.4 mW/channel**

The test power consumption of 5 channel Analog Front-end：2.02 mW/channel

Linearity Simulation of Analog Front-End

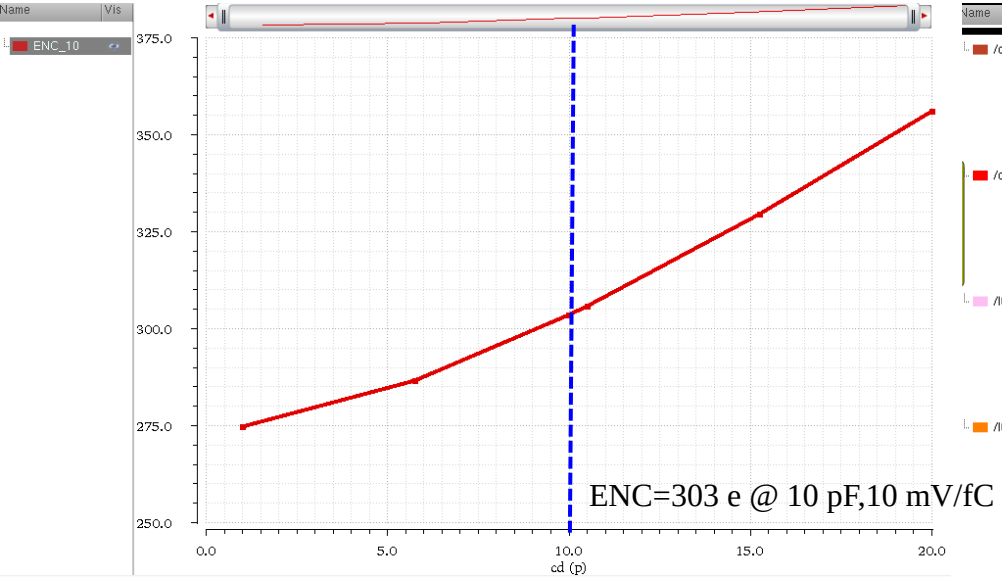




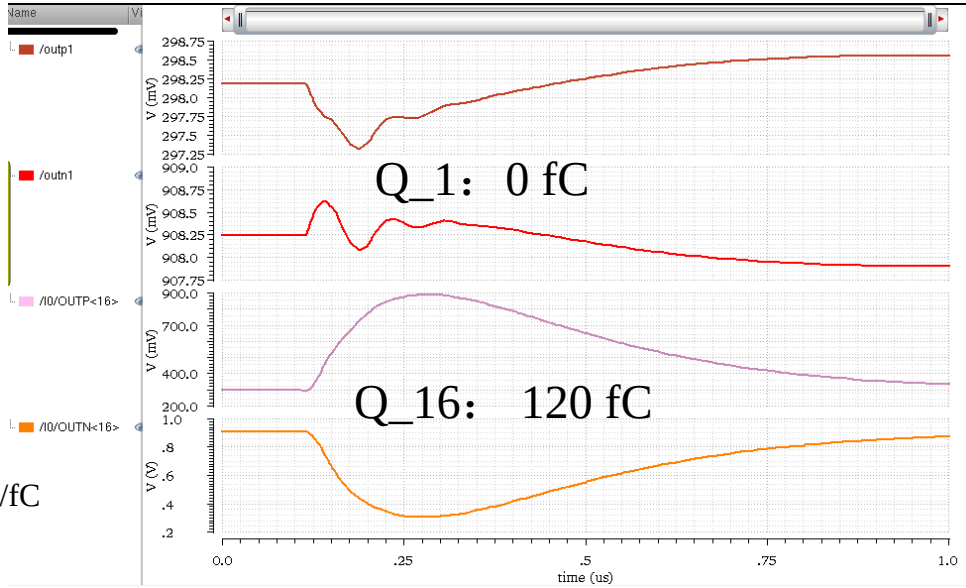
Gain(design value） mV/fC	10	20	30	40
Gain（simulation value） mV/fC	9.9	19.5	29.2	39.2

ENC and Crosstalk Simulation of Analog Front-End

- ENC



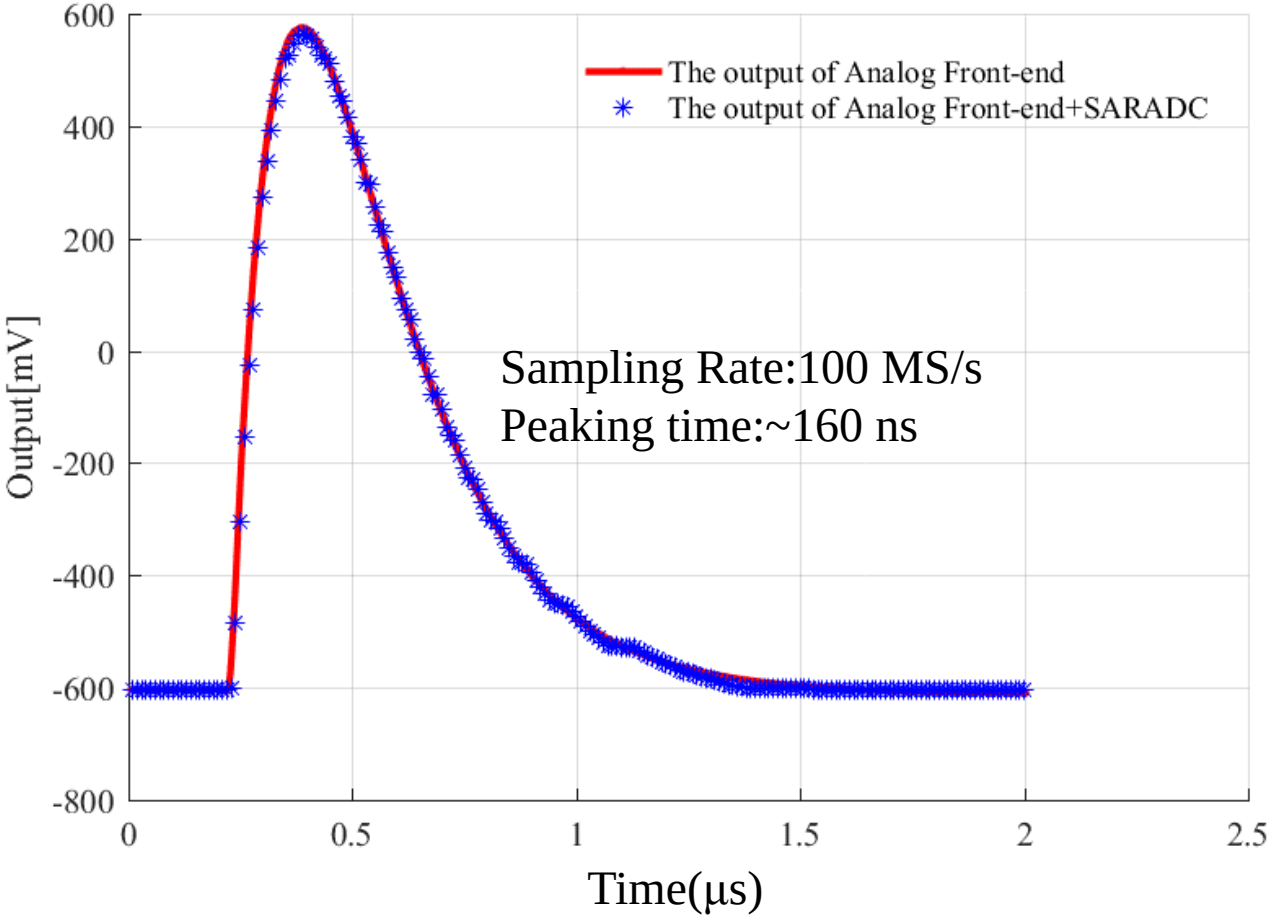
- Crosstalk



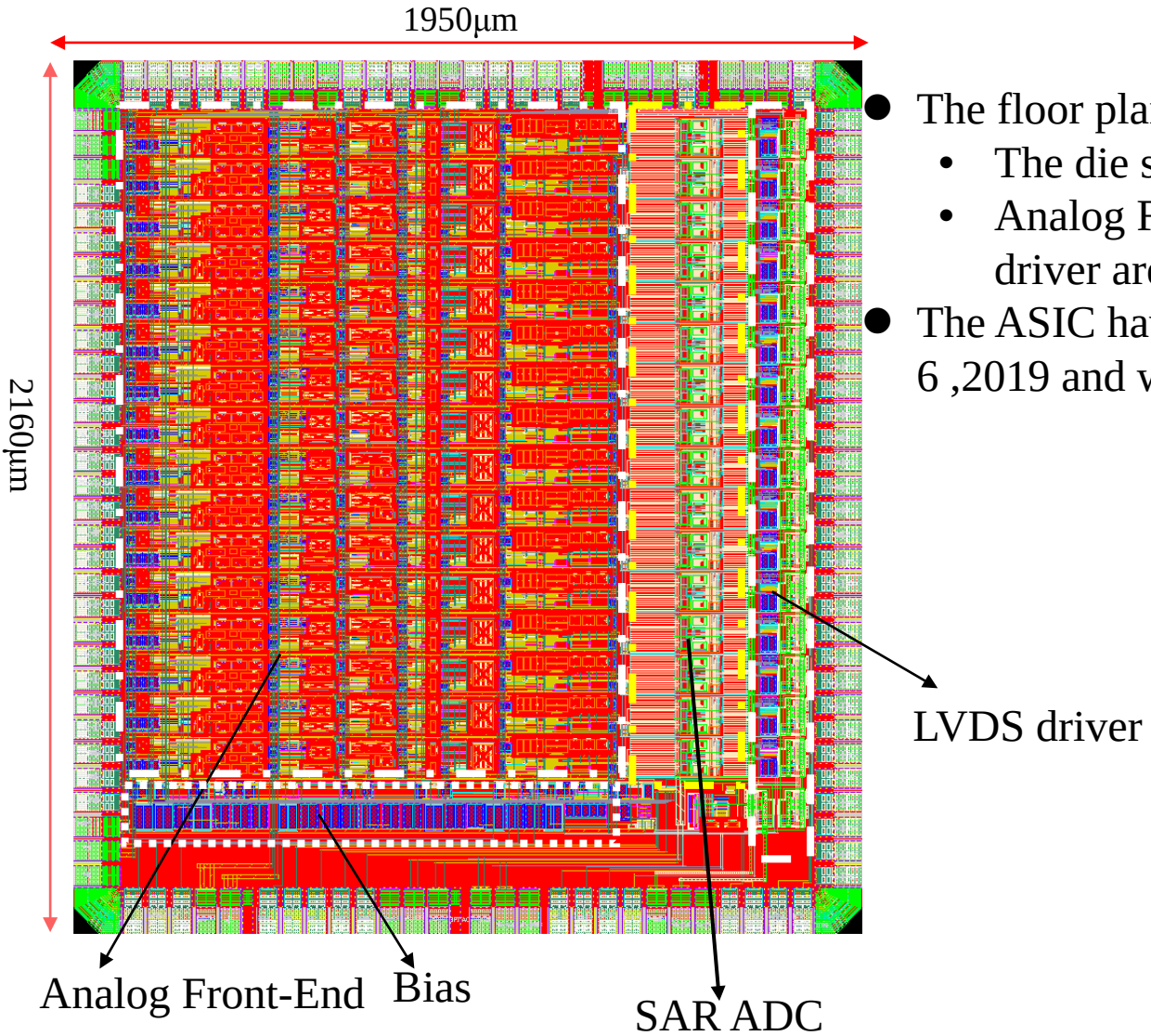
Gain mV/fC	10	20	30	40
ENC e @10 pF	303	189	159	146

Crosstalk： $\frac{1.526\ \mathrm{m}V}{1196\ mV} = 0.12\% < 1\%$

Transient Simulation of TPC Readout ASIC

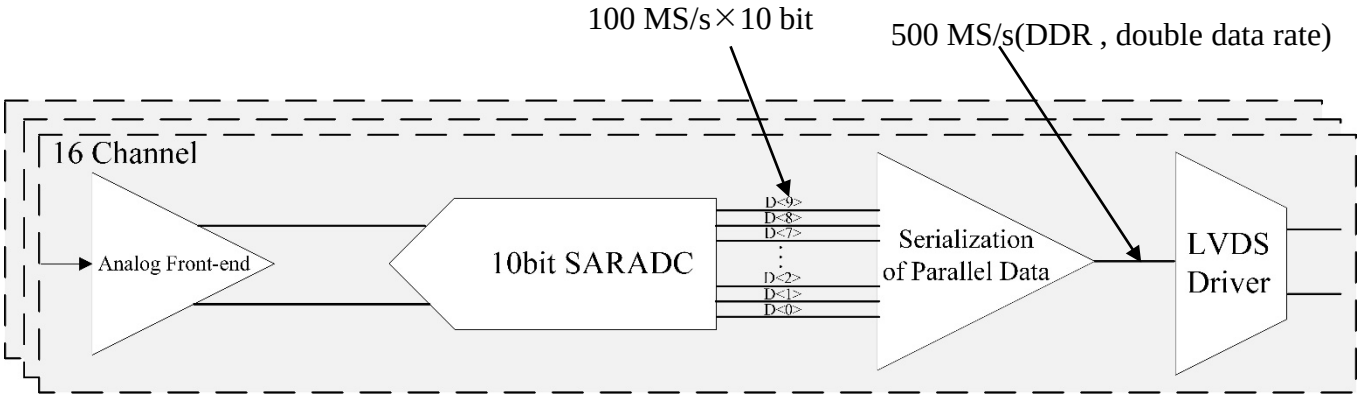


Layout of 16-ch TPC Readout ASIC



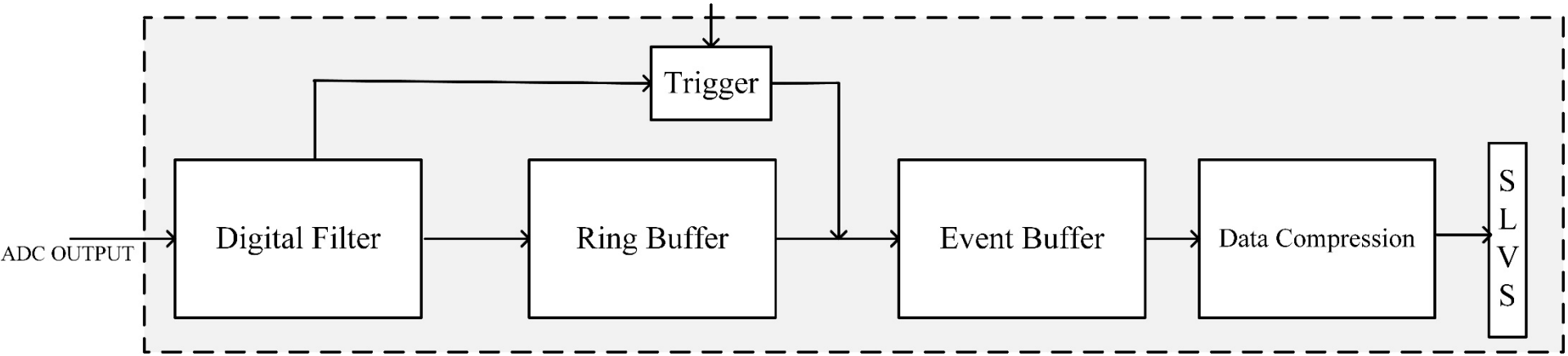
- The floor plan in layout：
  - The die size of 1950 μm x 2160 μm
  - Analog Front-End , SPI, SAR ADC, LVDS driver are supplied by separate power
- The ASIC have been taped out in November 6 ,2019 and will be evaluated in February,2020.

Digital Filter and Data Compression



- The drawback of ADC data direct output:
  - Pile up due to the long decay tail of CR-RC shaper
  - The high data rate from LVDS driver
  - The high power consumption of LVDS driver
- The solution:
  - Digital trapezoidal filter balances the ballistic deficit and pile up
  - Compress the data via zero suppression , Huffman suppression , etc

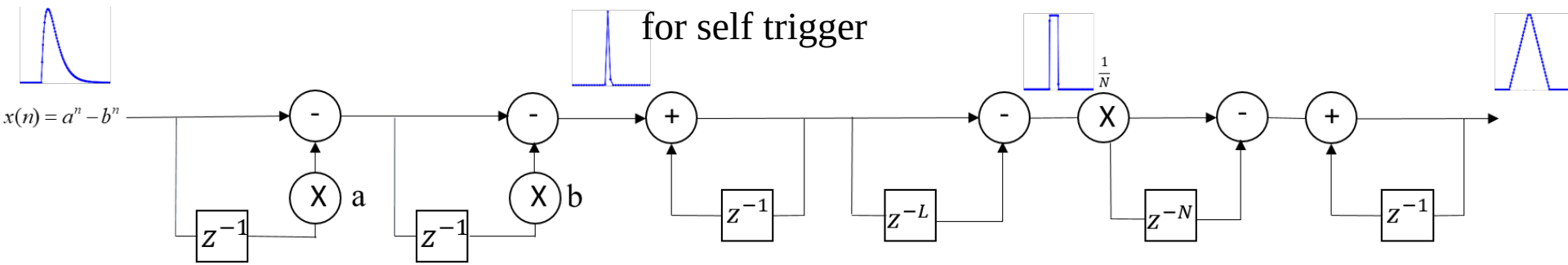
Preliminary Block Diagram of Digital Filter and Data Compression



Operating mode:

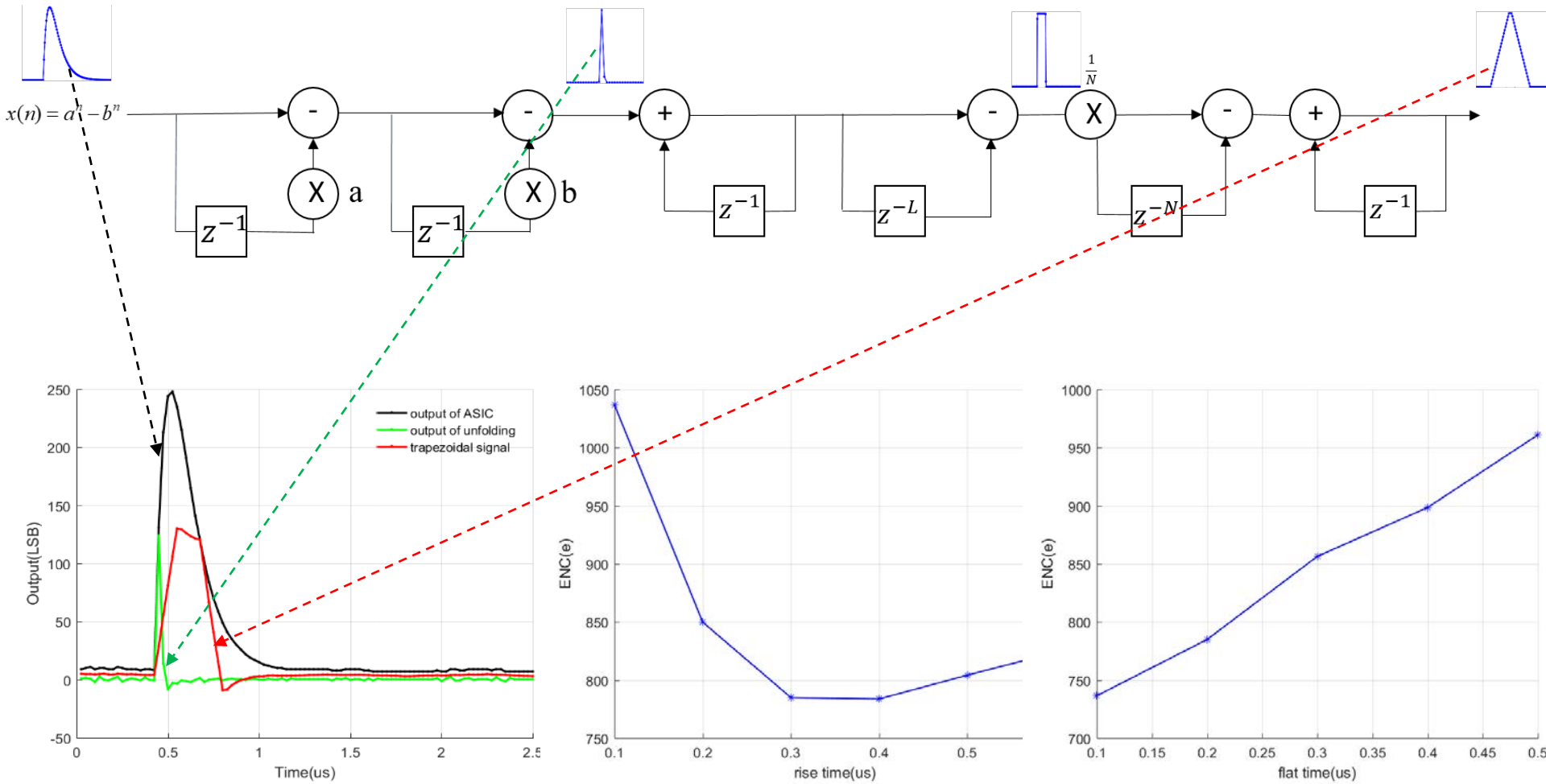
- Trigger mode: external trigger and self trigger
- Continuous operation

Digital Trapezoidal Filter



- The ballistic deficit can be avoided when the flat top is longer than detector charge collection time
- The waveform is symmetric, can achieve high SNR(signal to noise ratio)
- Hardware resource is low cost, can be well implemented on chip
  - 2 MUL (multiplications)
  - 6 ADD (additions) and SUB (subtractions)
  - some shift operations

Digital Trapezoidal Filter in MATLAB



When the flat top and rise time are suitable, the ENC can achieve minimum.

Summary

- 16 channel low power consumption and high integration ASIC for TPC readout have been developed
  - Based on the prototype ASICs of the first MPW run
  - adopting CR-RC shaper， achieving the analog part power consumption of 1.4 mW/channel, ENC:303 e @10 pF,10 mV/fC,
  - Adopting SAR ADC, achieving the core power consumption of 1 mW/channel，ENOB:9.2 bit @50 MS/s

Future Plan

- The evaluation of the 16 channel lower power and high integration ASIC using signal generator and TPC prototype
- Development of the full function CEPC TPC readout ASIC
  - Low power digital filter and data compression in FPGA
  - Full function ASIC including AFE,SARADC,DSP design

Thank You