中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

Design of the Pixel Analog

Ying ZHANG

30 April 2019, Chip design review on CEPC Vertex Detector of MOST2 project

Specifications of Pixel Cell

- **Spatial resolution: 3-5 μm (MOST2)**
  - Pixel size: < = 25 μm × 25 μm
  - Expect to be smaller for the final goal (2.8 μm for final CEPC innermost layer)

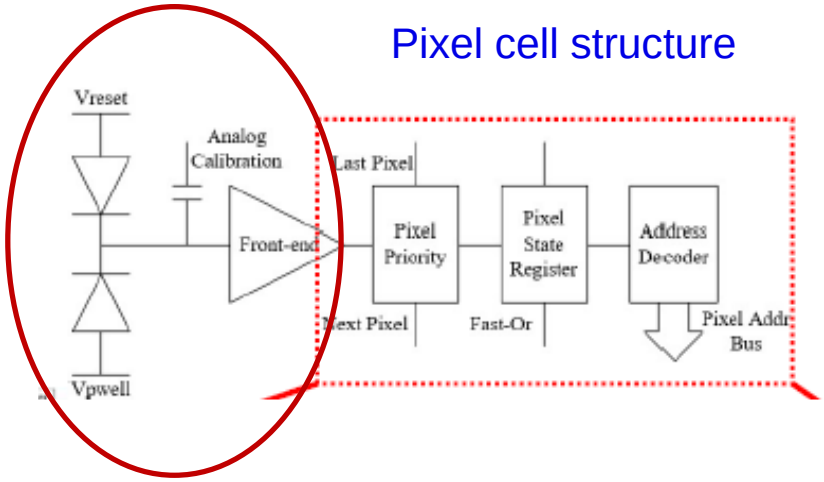
  ➔ **compact structure and layout**

- **Power density < 200 mW/cm²**
  - must work continuously

  ➔ **Low static current of front-end**

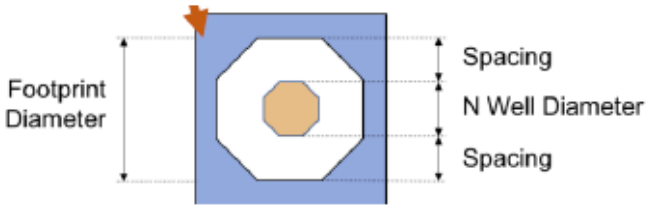
- **Minimum bunch spacing 25 ns**
  - Time stamp of the hit is added at EOC ➔small Time walk (time difference between bunch crossing time and leading edge of hit pixel signal)

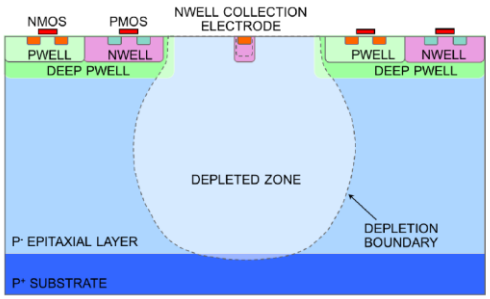
Pixel cell structure



Design of Sensor

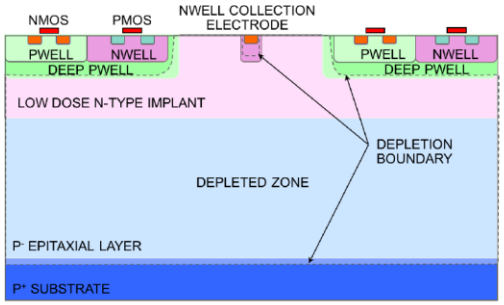
- **Goal: high Q/C (collected charge/sensor capacitance)**
  - **Small collection electrode → low C**
  - **High charge collection efficiency → high Q**
- **Process options:**
  - High resistivity sensitive layer (> 1 kΩ cm)
  - Deep p-well shielding n-well to allow full CMOS





Baseline process

no full depletion on pixel edges



Modified process

additional low doped n-layer

full depletion, faster charge coll. & better rad. tolerance

W. Snoeys et al.
DOI 10.1016/j.nima.2017.07.046

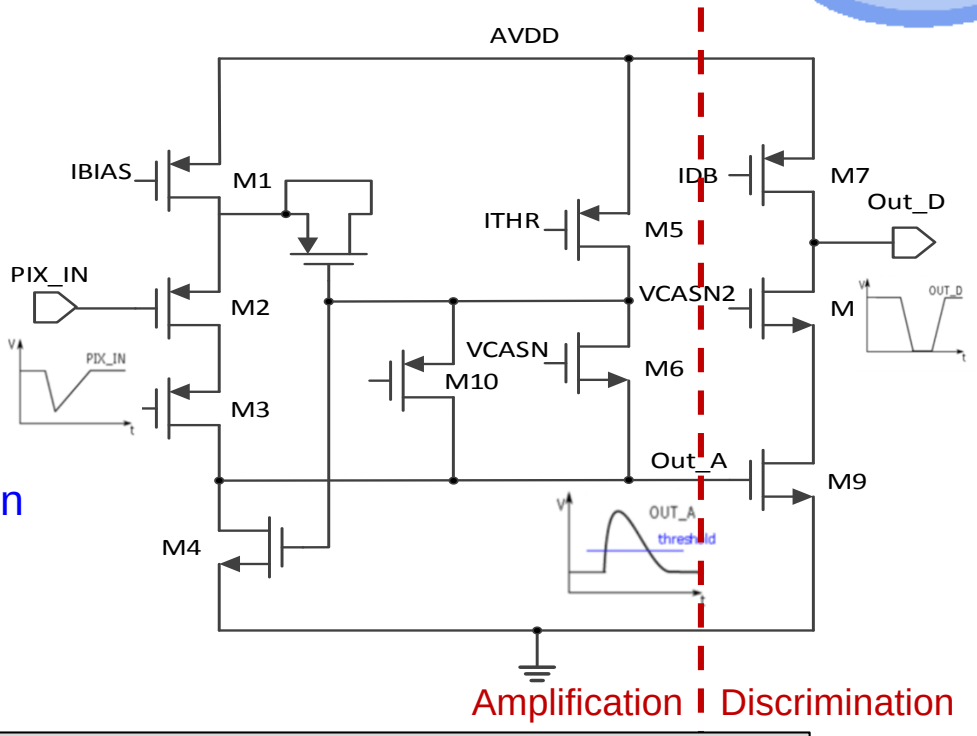
- **Design key points**
  - **Diode geometry optimization**, benefit from previous design (JadePix1)
    - 2-3 μm small electrode & large footprint
  - **Reverse bias** (~ 6V) ➔ reduce C & increase depletion volume

Schematic of Front-end

- **Operating principle derived from ALPIDE front end**

  D. Kim et al. DOI 10.1088/1748-0221/11/02/C02042

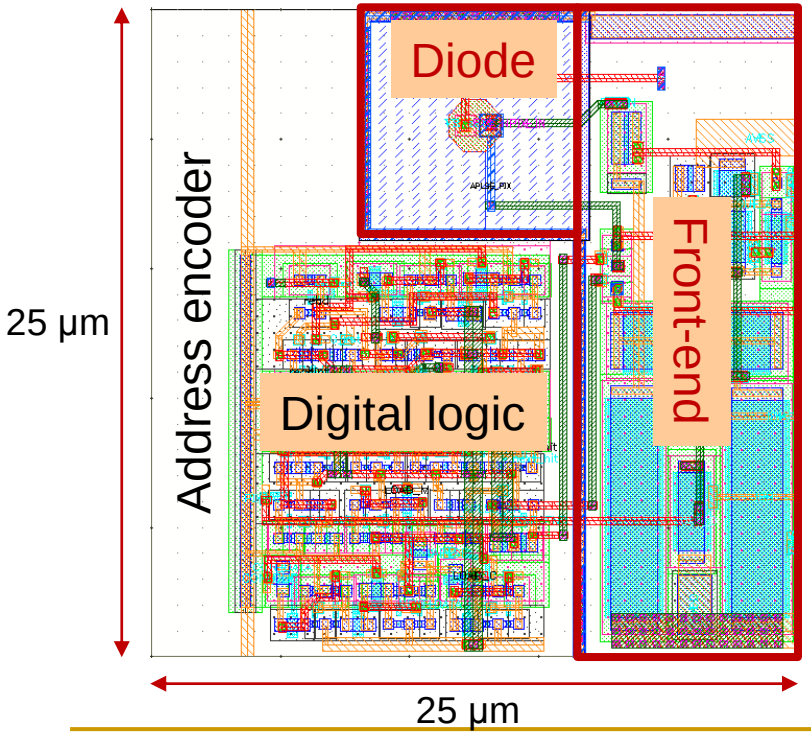
- **Modification for fast timing response**
  - at the cost of power consumption
- **Reduction on layout area**
- **Low threshold disp.**

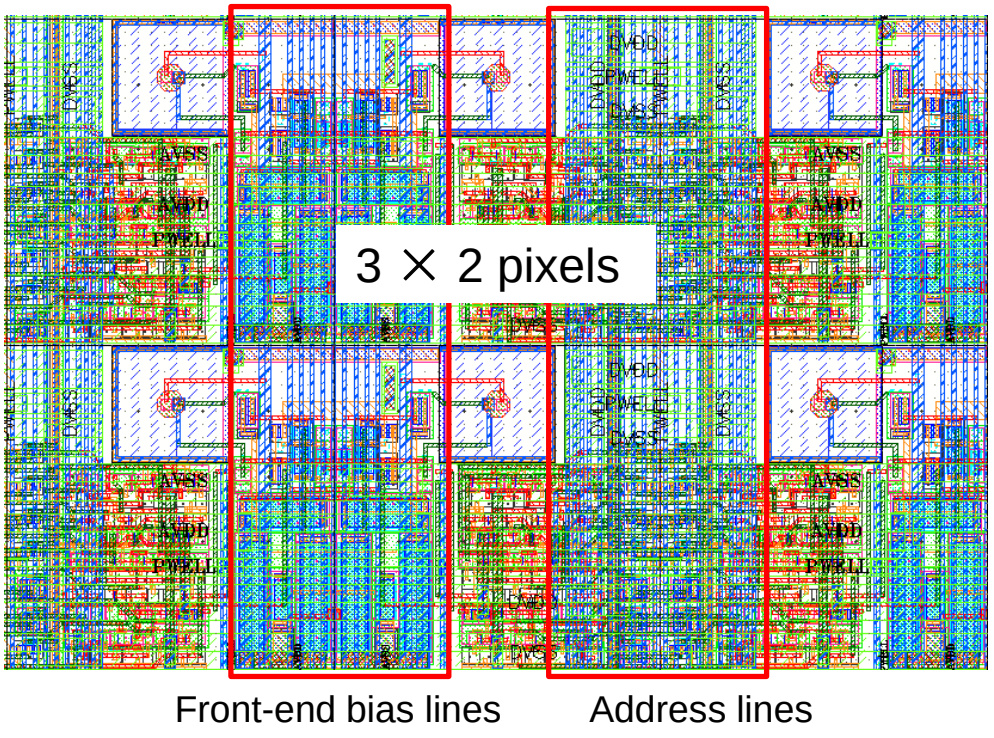


- M2 acts as a source follower to avoid loading the input
- M3 is a cascode transistor to increase the gain on the output node and eliminate the Miller effect for the input node.
- The analog output node is stabilized at low frequencies by active feedback on the transistor M4
- Efficient current usage for the input (the same branch current powers the source follower and the amplification stage)
- M10: clipping of the analog pulse

Layout

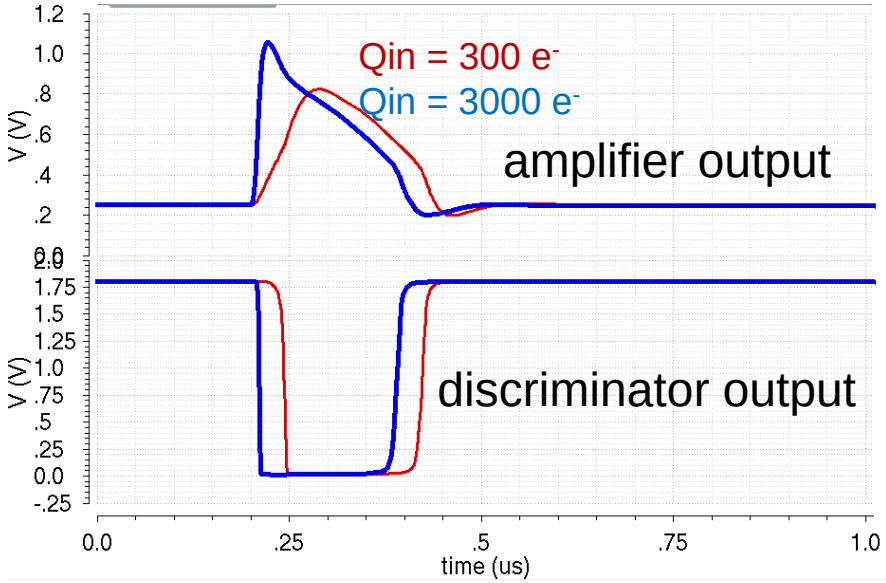
- **Pixel size: 25 μm × 25 μm**
  - Sensor + Front-end occupy 45% pixel area
    - Smaller area possible
  - Shield from digital part to minimize crosstalk
  - Pixels are aside to separate analog and digital part
  - Two adjacent pixel analog share biasing signal routing

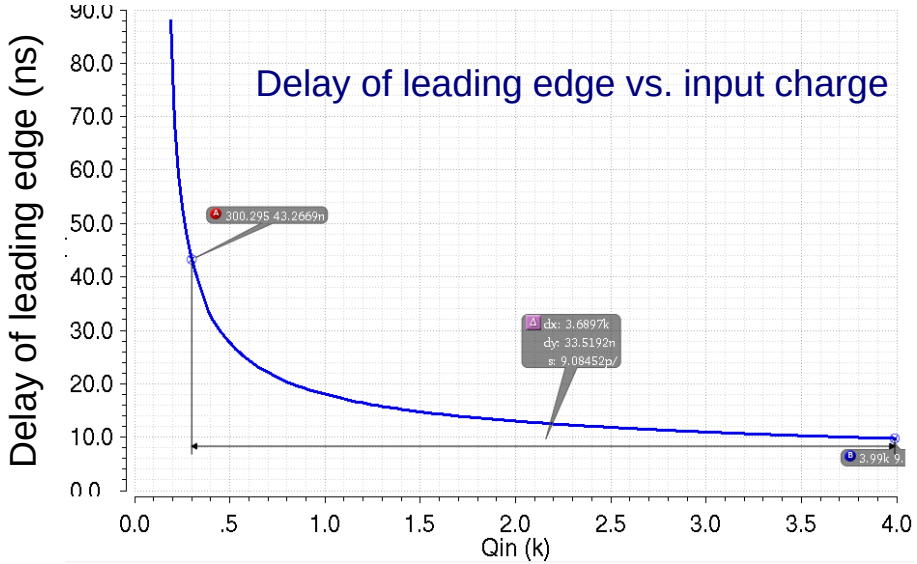




Front-end simulation result (1)

- **Transient simulation:**
  - Post simulation with parasitic RCC of the front-end
  - Analog power consumption 130 mW/cm^2
  - Duration time (discriminator output) < 200 ns
  - Time walk: time difference between time over threshold
    - ~33 ns @ 300e – 4 ke-

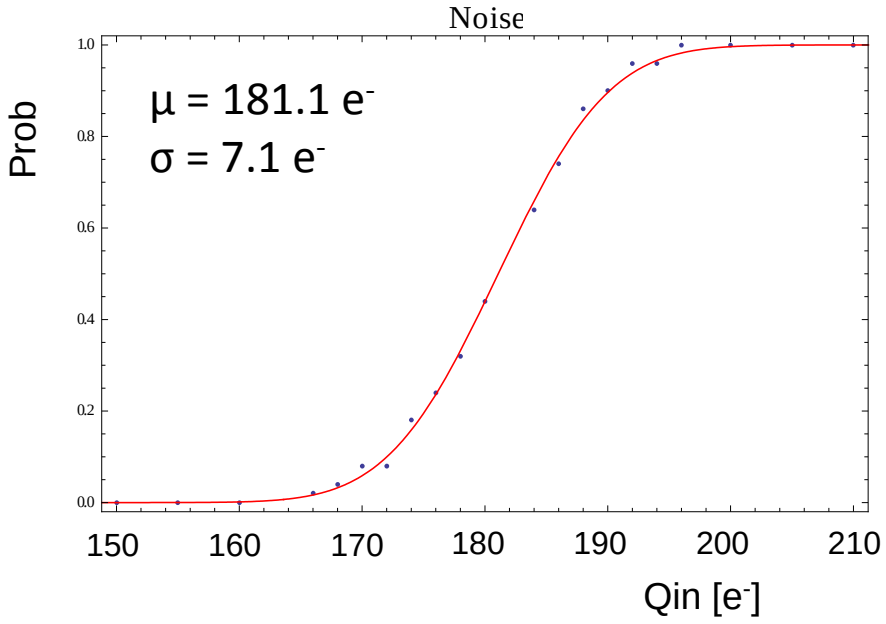


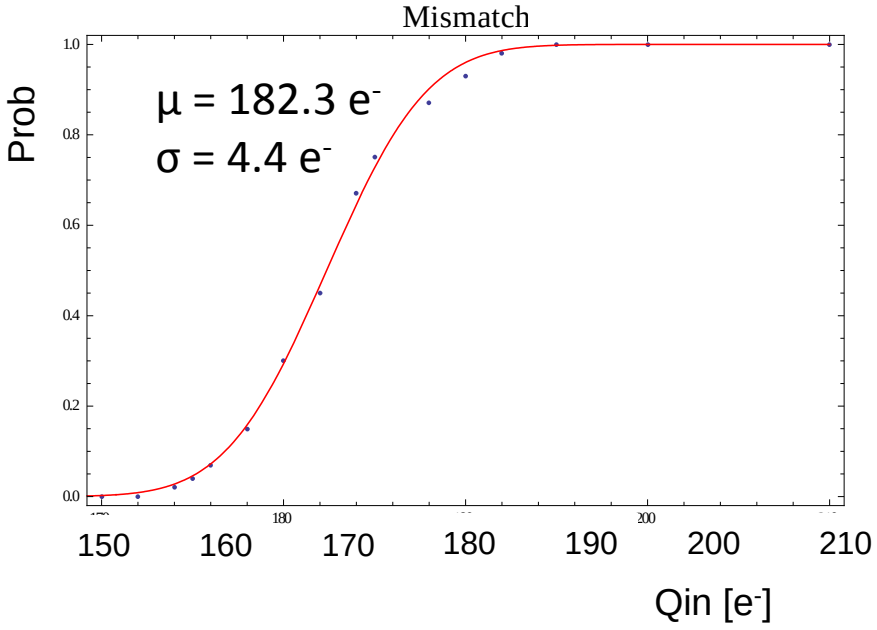


Front-end simulation result (2)

- **Equivalent noise charge and threshold dispersion:**
  - Transient noise simulation with different input charges, 50 runs for each input, record number of “hit” → “S curve”

  ➔ Charge threshold 181 e-, Equivalent noise charge: 7.1 e-
- **Threshold dispersion:**
  - Monte Carlo simulation (mismatch) with different input charges, 100 runs for each input ➔ threshold dispersion 4.4 e^-





Summary

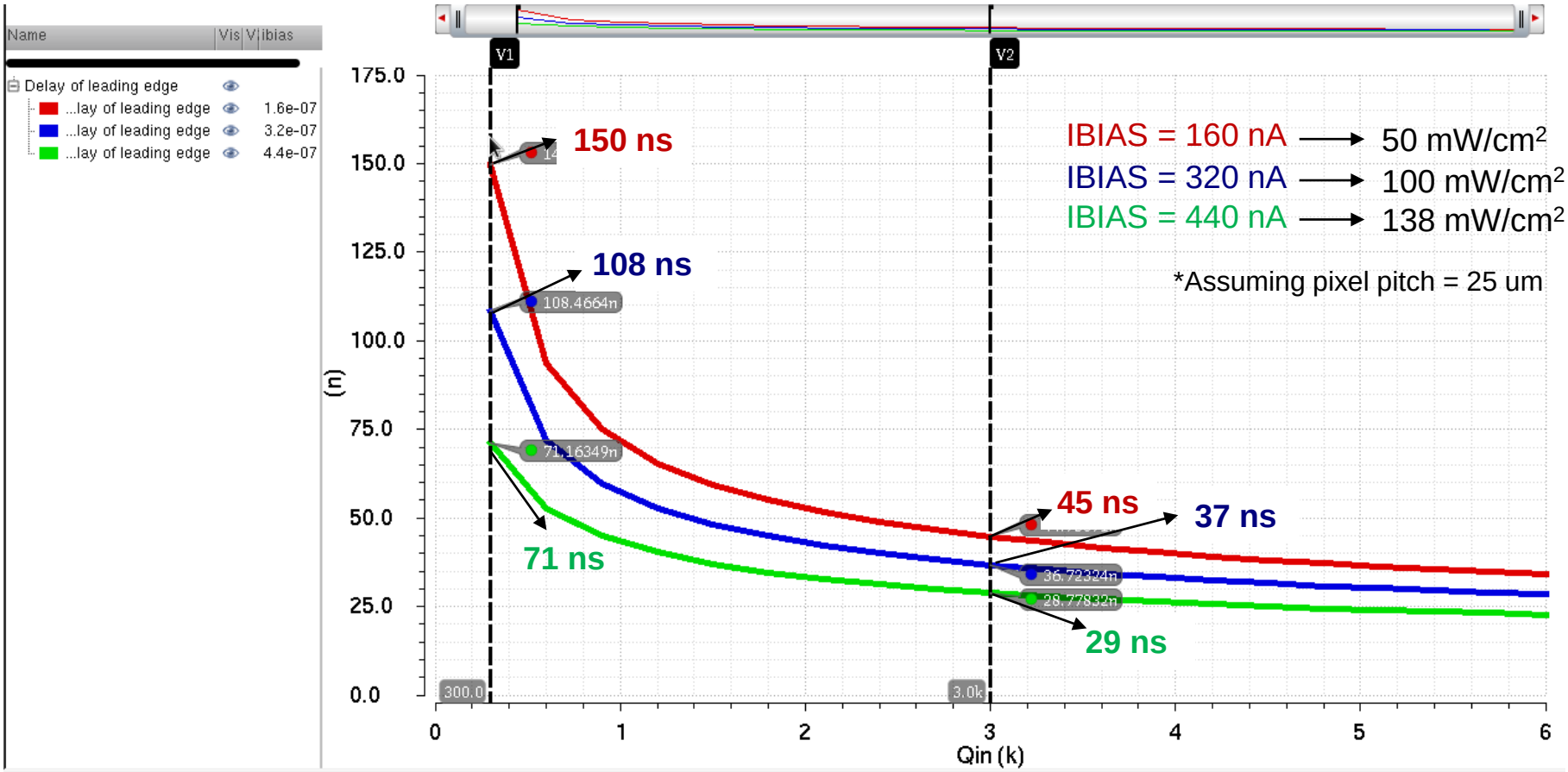
- A fast, compact pixel analog designed
- Preliminary post-simulation results satisfy the specs.
- Simulation and further optimization in progress

Thanks for your attention !

Backup slides

Time walk vs. power consumption

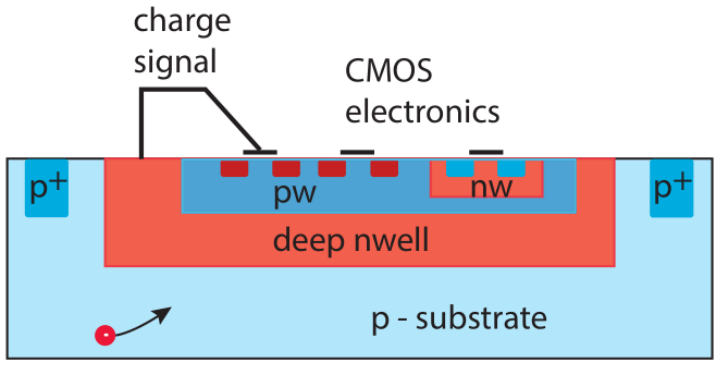
Delay of leading edge vs. input charge



300 e⁻ 3000 e⁻

CMOS sensors: Large vs. Small collection electrode

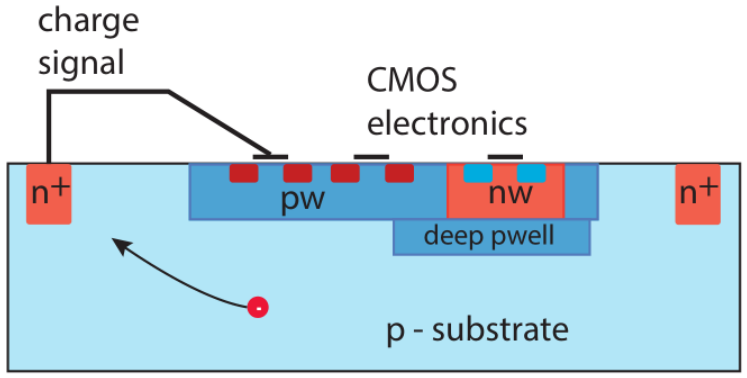
Large collection electrode



M. Garcia-Sciveres and N. Wermes, arXiv:1705.10150

- Larger capacitance: $C \approx 300 - 400$ fF
- Higher analog power, sensitive to crosstalk
- Uniform, strong drift field, high radiation tolerance and detection efficiency

Small collection electrode



- Smaller capacitance: $C \approx 3$ fF → low power
- Less sensitive to crosstalk
- Longer drift paths
- Full depletion can be achieved by modifying the process → radiation tolerance increases

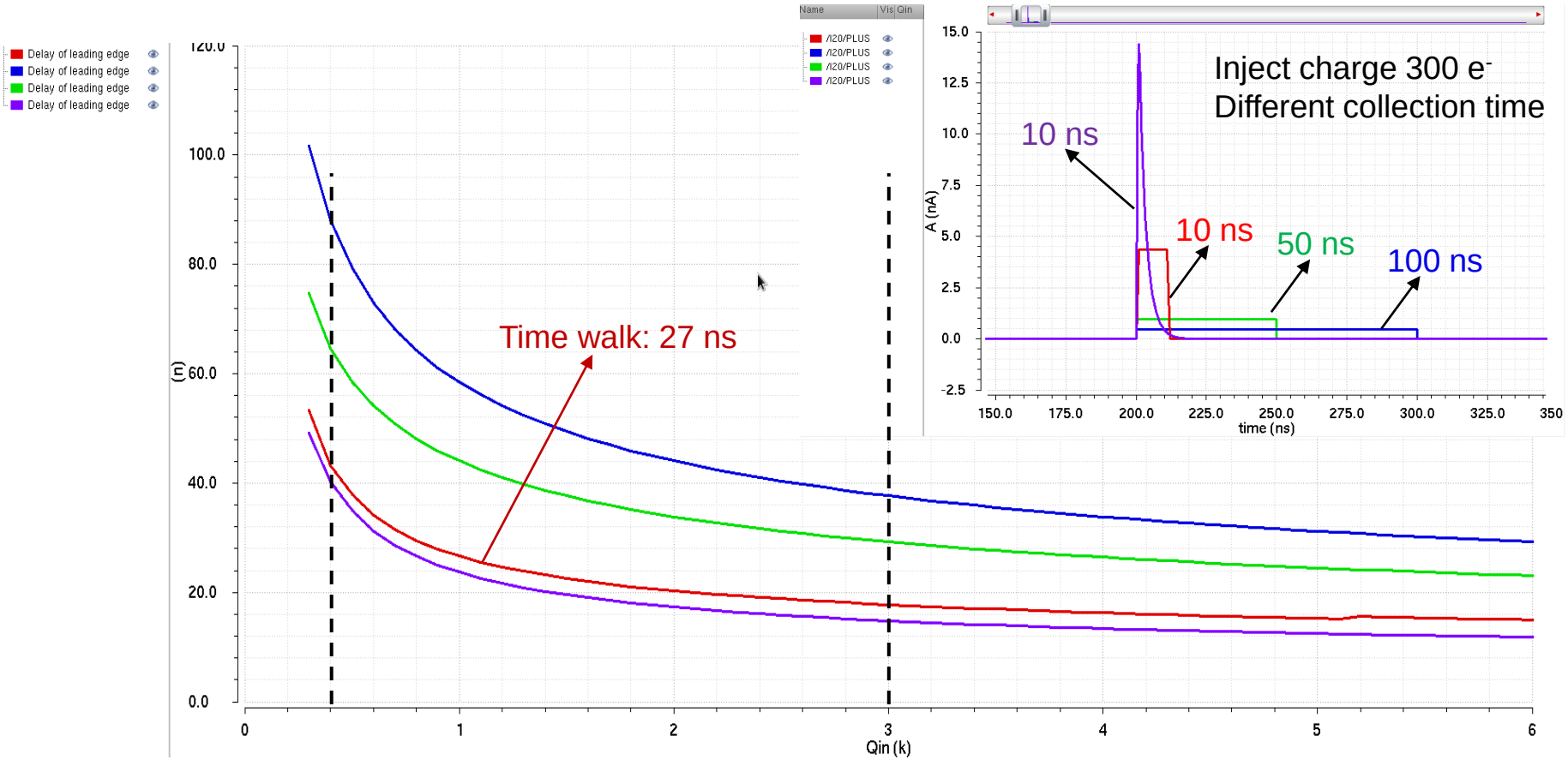
$$\tau_{\mathrm{CSA}} = \frac{1}{g_{\mathrm{m}}}\frac{C}{C_{\mathrm{f}}} \qquad ENC^2_{\mathrm{thermal}} = \frac{4}{3}\frac{kT}{g_{\mathrm{m}}}\frac{C^2}{\tau_{\mathrm{f}}} \qquad \frac{S}{N} \approx \frac{Q/C}{\sqrt{g_{\mathrm{m}}}} \sim \frac{Q/C}{\sqrt[m]{P}} \Rightarrow P \sim \left(\frac{Q}{C}\right)^{-m}$$

B. Hiti et al. Development of the monolithic "MALTA" CMOS sensor for the ATLAS ITK out pixel layer TWEPP 2018

Front-end simulation

Simulation condition: Cd = 2.5 fF, IBIAS = 440 nA

Delay of leading edge vs. input charge vs. charge collection time



Time walk increases with collection time