Chip Design Review for the MPW1 of the CEPC MOST2 Vertex Detector -- Overview

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On behalf of the CEPC MOST2 Vertex detector design team

2019-4-30

Purpose of this design review meeting

- **Review the overall scheme of the chip**
- **Review the readout architecture feasibility**
- **Review the detailed design especially on the pixel cell, and periphery logic**
- **General status of other periphery blocks**

Outline

- **Specification of the CEPC Vertex Detector and Chip Design**
- **Main scheme and modification for the high-rate & fine pitch Vertex Detector**
- **Overview of the preliminary design**

CEPC Vertex Detector Design

Detector Requirements

- Efficient tagging of heavy quarks (b/c) and τ leptons

  ⟶ impact parameter resolution

$$\sigma_{r\phi} = 5 \oplus \frac{10}{p(GeV)\,\sin^{3/2}\theta}\,(\mu m)$$

- Detector system requirements:
  - σ_{SP} near the IP: *<3 μm* ⟶ ~16μm pixel pitch
  - material budget: *≤ 0.15%X $_0$/layer* ⟶ power consumption < 50mW/cm^2 , if air cooling used
  - first layer located at a radius: *~1.6 cm*
  - pixel occupancy: *≤ 1 %* ⟶ ~ μs level readout

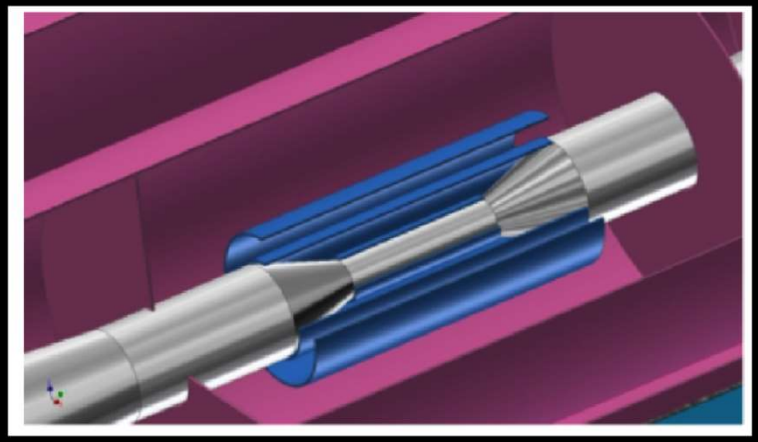
Target: fine pitch, low power, fast pixel sensor + light structure

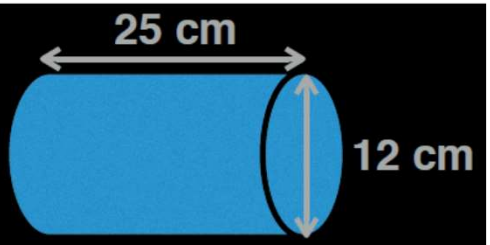
- **Ref: Status of vertex detector, Q. Ouyang, International workshop on CEPC, Nov. 7th 2017**

Baseline Vertex Detector design

Baseline Pixel Detector Layout

3-layers of double-sided pixel sensors



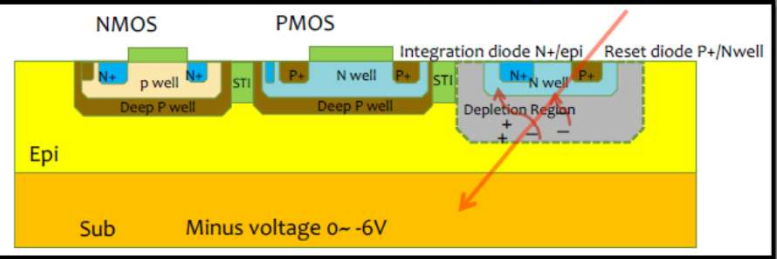


- ILD-like layout
- Innermost layer: σ_{SP} = 2.8 μm
- Polar angle θ ~ 15 degrees

Implemented in GEANT4 simulation framework (MOKKA)

		$R(mm)$	$\|z\|(mm)$	$\|cos\theta\|$	$\sigma(\mu m)$	$Readout\ time(us)$
Ladder 1	Layer 1	16	62.5	0.97	2.8	20
	Layer 2	18	62.5	0.96	6	1-10
Ladder 2	Layer 3	37	125.0	0.96	4	20
	Layer 4	39	125.0	0.95	4	20
Ladder 3	Layer 5	58	125.0	0.91	4	20
	Layer 6	60	125.0	0.90	4	20

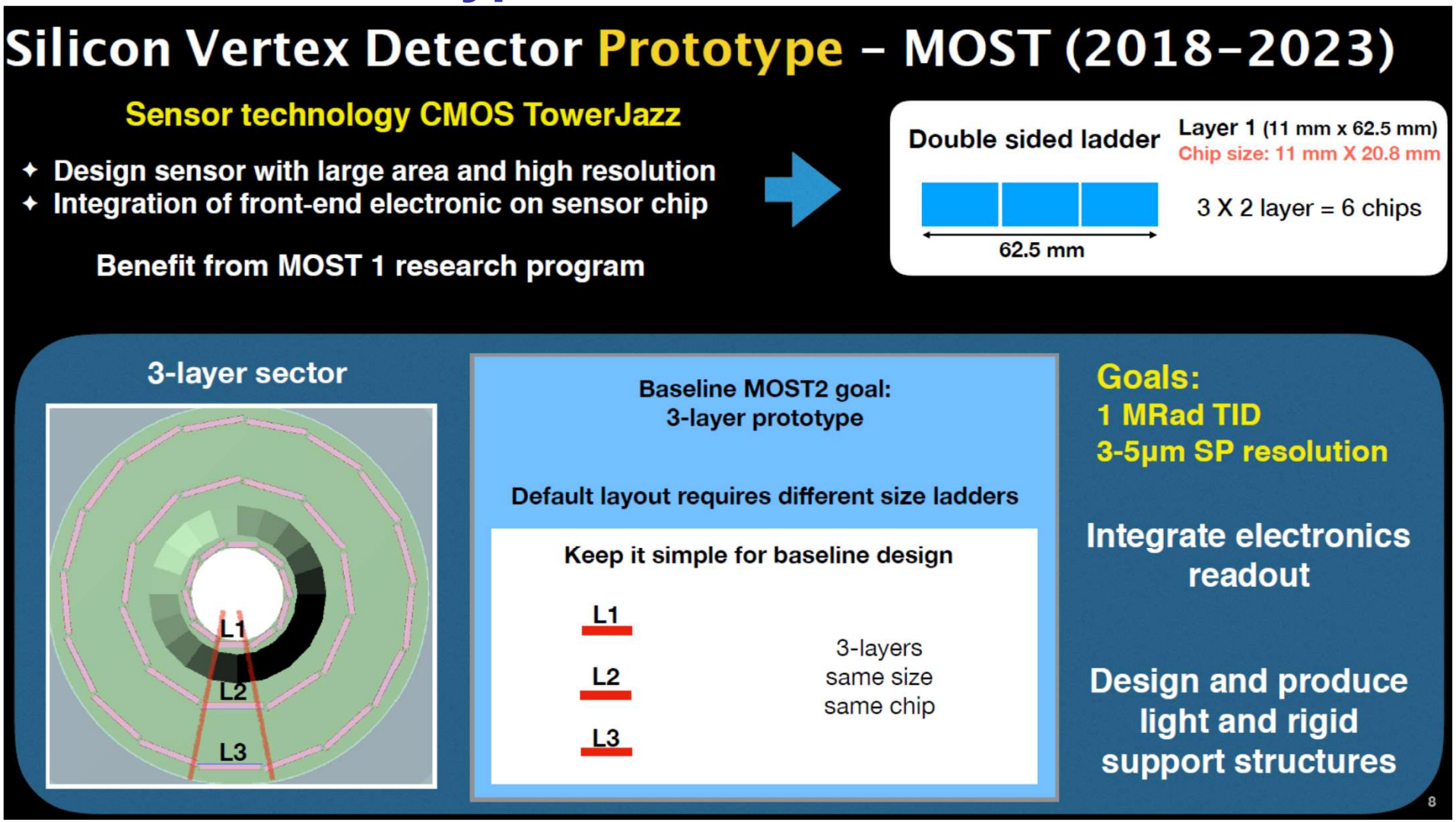
CMOS pixel sensor (MAPS)



Integrated sensor and readout electronics on the same silicon bulk with "standard" CMOS process:
- low material budget,
- low power consumption,
- low cost …

- Ref: Introduction to the Pixel MOST2 Project, Joao Costa, 2018.6

Ladder Prototype



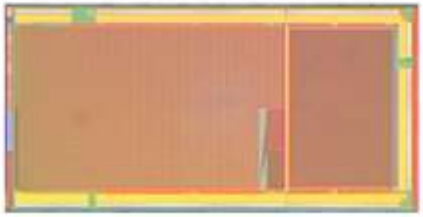
- **Motivation for chip design:**
  - **Full size, full functional chip**
  - **Assembled on ladders with backend Elec. & DAQ**

- **Ref: Introduction to the Pixel MOST2 Project, Joao Costa, 2018.6**

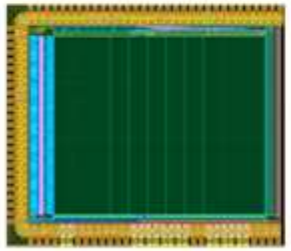
Previous studies from MOST1

Prototype	Pixel pitch (μm^2)	Collection diode bias (V)	In-pixel circuit	Matrix size	R/O architecture	Status
JadePix1	33 × 33 16 × 16	< 1.8	SF/amplifer	96 × 160 192 × 128	Rolling shutter	In measurement
JadePix2	22 × 22	< 10 V	amp., discriminator	128 × 64	Rolling shutter	In measurement
MIC4	25 × 25	reverse bias	amp., discriminator	112 × 96	Asynchronous	In measurement

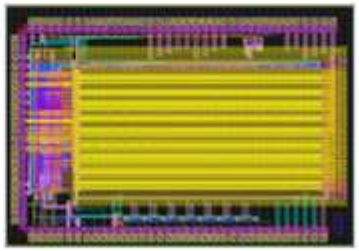
- **all prototypes in Towerjazz 180nm process**



JadePix1 (IHEP)
3.9 × 7.9 mm^2



JadePix2 (IHEP)
3 × 3.3 mm^2



MIC4 (CCNU & IHEP)
3.2 × 3.7 mm^2

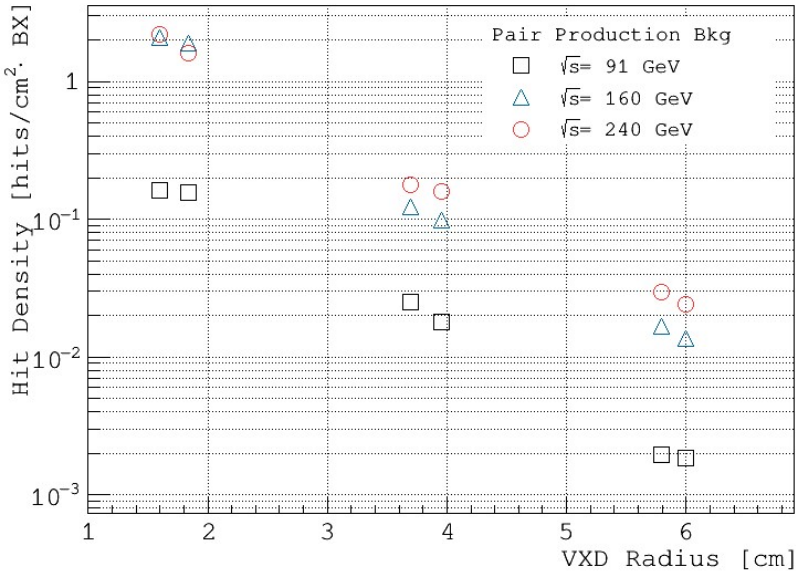
- **Slides from Y. Zhang: "IHEP CMOS pixel sensor activities for CEPC", 2018.3**
- **Y.P. Lu, The 2018 International Workshop on the High Energy Circular Electron Positron Collider**

- **Chip design baseline approach:**
- **Key component based on MOST1： sensing diode + Pixel Analog**
- **Necessary modification on readout architecture**

Main specs of the full size chip for high rate vertex detector

- **Bunch spacing**
  - **Higgs: 680ns; W: 210ns; Z: 25ns**
  - **Meaning 40M/s bunches (same as the ATLAS Vertex)**
- **Hit density**
  - **2.5hits/bunch/cm^2 for Higgs/W; 0.2hits/bunch/cm^2 for Z**
- **Cluster size: 3pixels/hit**
  - **Epi- layer thickness：~18μm**
  - **Pixel size：25μm×25μm**

From the CDR of CEPC

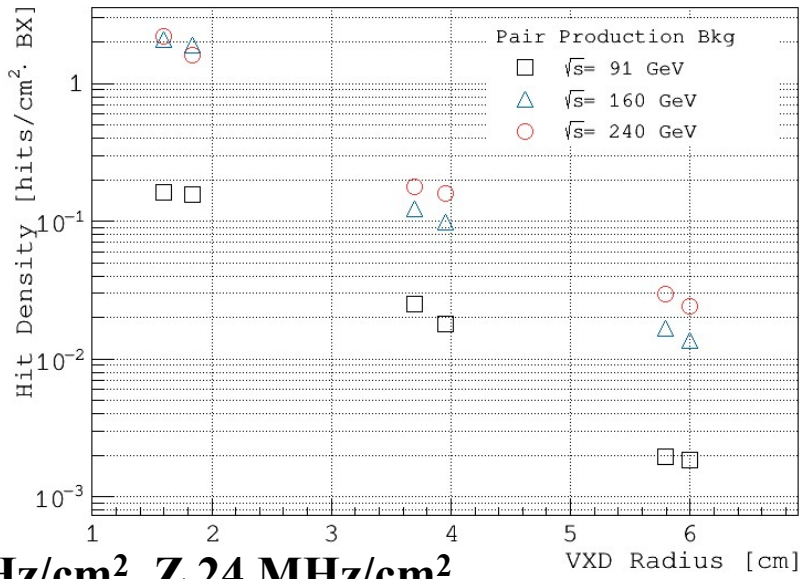


For Vertex	Specs	For High rate Vertex	Specs	For Ladder Prototype	Specs
Pixel pitch	<25μm	Hit rate	120MHz/chip	Pixel array	512row×1024col
TID	>1Mrad	Date rate	3.84Gbps --triggerless ~110Mbps --trigger	Power Density	< 200mW/cm^2 (air cooling)
		Dead time	<500ns --for 98% efficiency	Chip size	~1.4cm×2.56cm

Discussions for main specs of MOST2 chip

- **Bunch spacing**
  - **Higgs: 680ns; W: 210ns; Z: 25ns**
  - **Meaning 40M/s bunches (design should count for the max)**
- **Hit density**
  - **2.5hits/bunch/cm^2 for Higgs/W; 0.2hits/bunch/cm^2 for Z**
- **Cluster size: 3pixels/hit**

From CDR of CEPC



- **The hit rate: Higgs 11 MHz/cm^2, W 36MHz/cm^2, Z 24 MHz/cm^2**
- **The chip should be capable with 36MHz/cm^2 hit rate**
- **Suppose the pixel array size is 512rows*1024cols (ALPIDE), 25um*25um pixel size, and 1.28cm*2.56cm pixel array area**
- **→ Hit rate: 120MHz/chip, or 225Hz/pixel (average), 120kHz/col (ave)**
  - **Meaning every 8.3us, the column will be hit, however, very unlikely to be at the same pixel**
- **Every hit has 27~32bits (async): col addr 9bits (512), row addr 10bits (1024), time stamp ~8bits (suppose 40MHz clock, covers 6.4us time region)**

Discussions for main specs of MOST2 chip

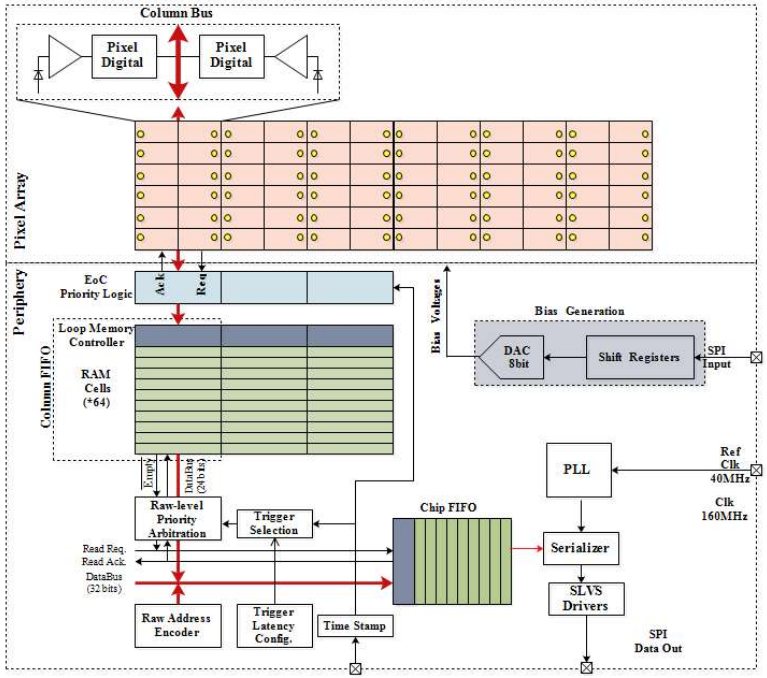
- **Every hit has 27~32bits (async): col addr 9bits (512), row addr 10bits (1024), time stamp ~8bits (suppose 40MHz clock, covers 6.4us time region)**
- **If triggerless, all the raw hit data should be sent off chip**
  - **The data rate: ~32bits*120MHz= 3.84Gbps, possible, but risk too high in the current stage**
- **If trigger, on-chip buffer should be designed**
  - **Suppose trigger latency 3us. Trigger rate was said 20kHz~50kHz**
  - **Triggered data rate:**
    - **2.5/hits/bunch/cm^2*3pixels/hit*1.28cm*2.56cm*32bit=786bit/bunch/chip**
    - **W@20kHz trigger rate -> 15.7Mbps/chip as the triggered data rate**
  - **In order to cover any trigger error(mismatch of the edge in different column, time walk of the hit peaking…)**
    - **A trigger window can be set, so that the data within the ±σ of the trigger time stamp can all be read out**
    - **In this way, the readout data rate will be (suppose trigger window of ±3LSB time stamp):**
      - **15.7Mbps * 7 ~ 110Mbps**
      - **Can still be read out by a single LVDS interface**

Limitation of the existing CMOS sensors

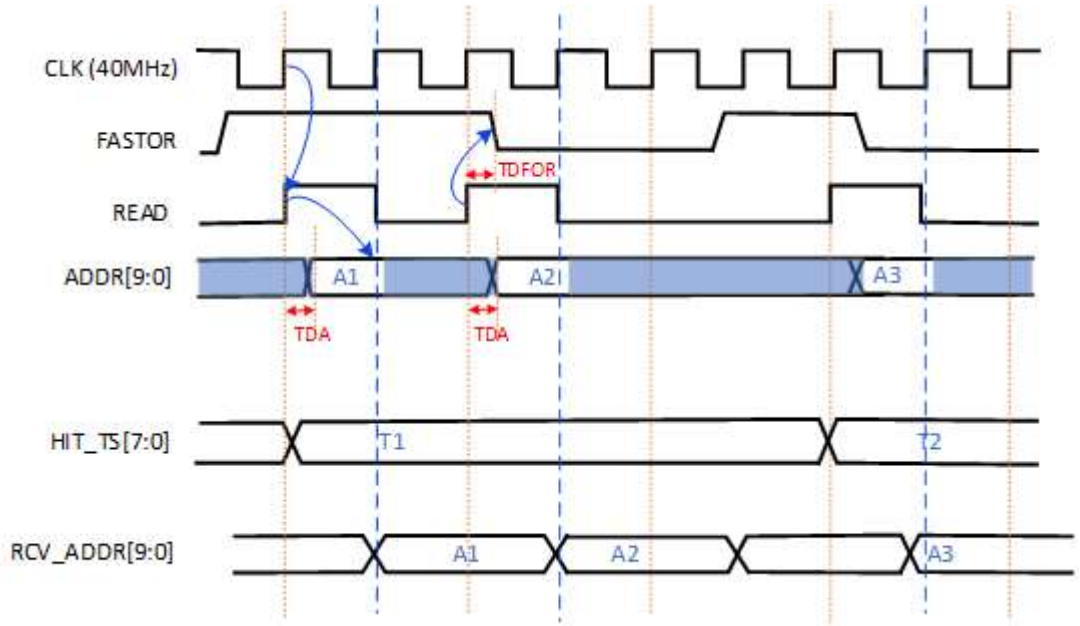
- **None of the existing CMOS sensors can fully satisfy the requirement of high-rate CEPC Vertex Detector**
- **Two major constraints for the CMOS sensor**
  - **Pixel size: should be < 25um* 25um, aiming for 16um*16um**
  - **Readout speed: bunch crossing @ 40MHz**
- **TID is also a constraint, but 1Mrad is not so difficult**

	ALPIDE	ATLAS-MAPS (MONOPIX / MALTA)	MIMOSA
Pixel size	✔	X	✔
Readout Speed	X	✔	X
TID	X (?)	✔	✔

New proposed architecture for MOST2

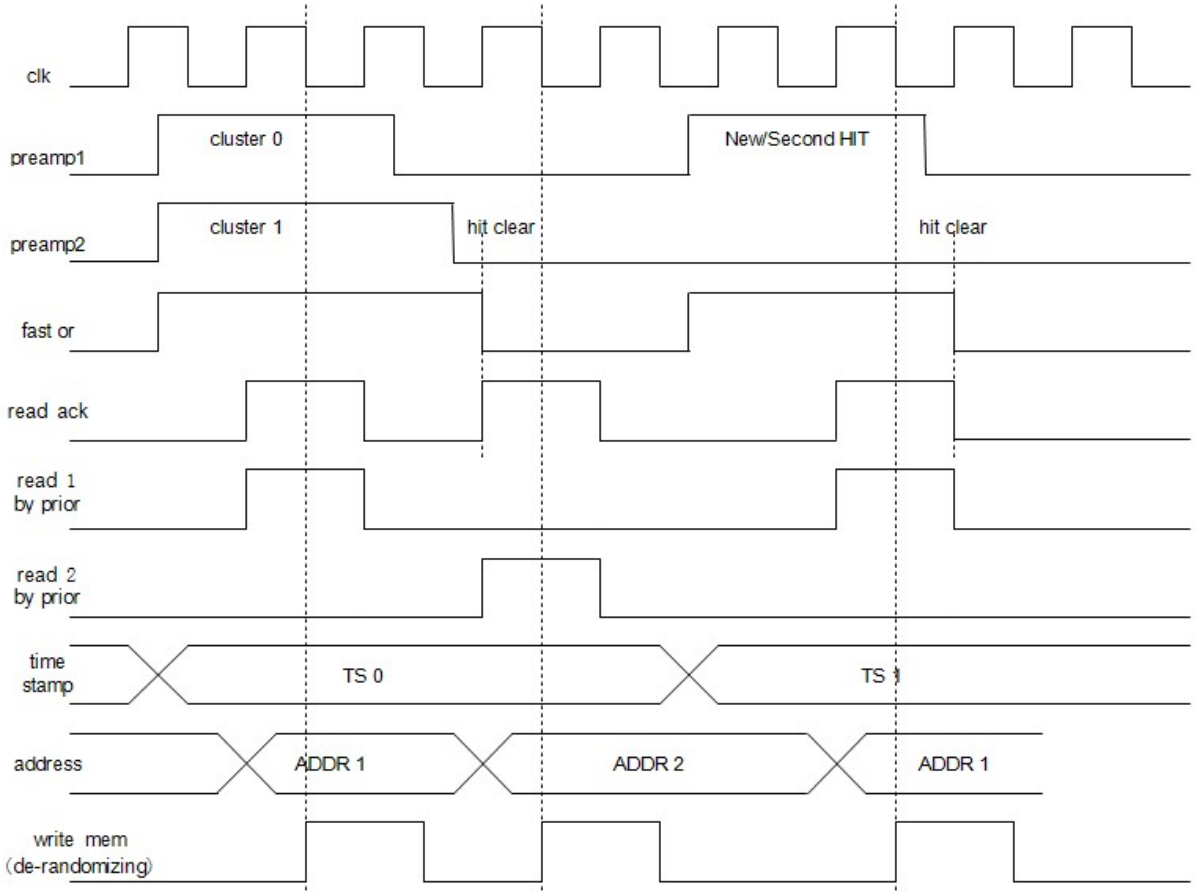


From X.M. Wei for the CEPC Vertex MOST2 group meeting



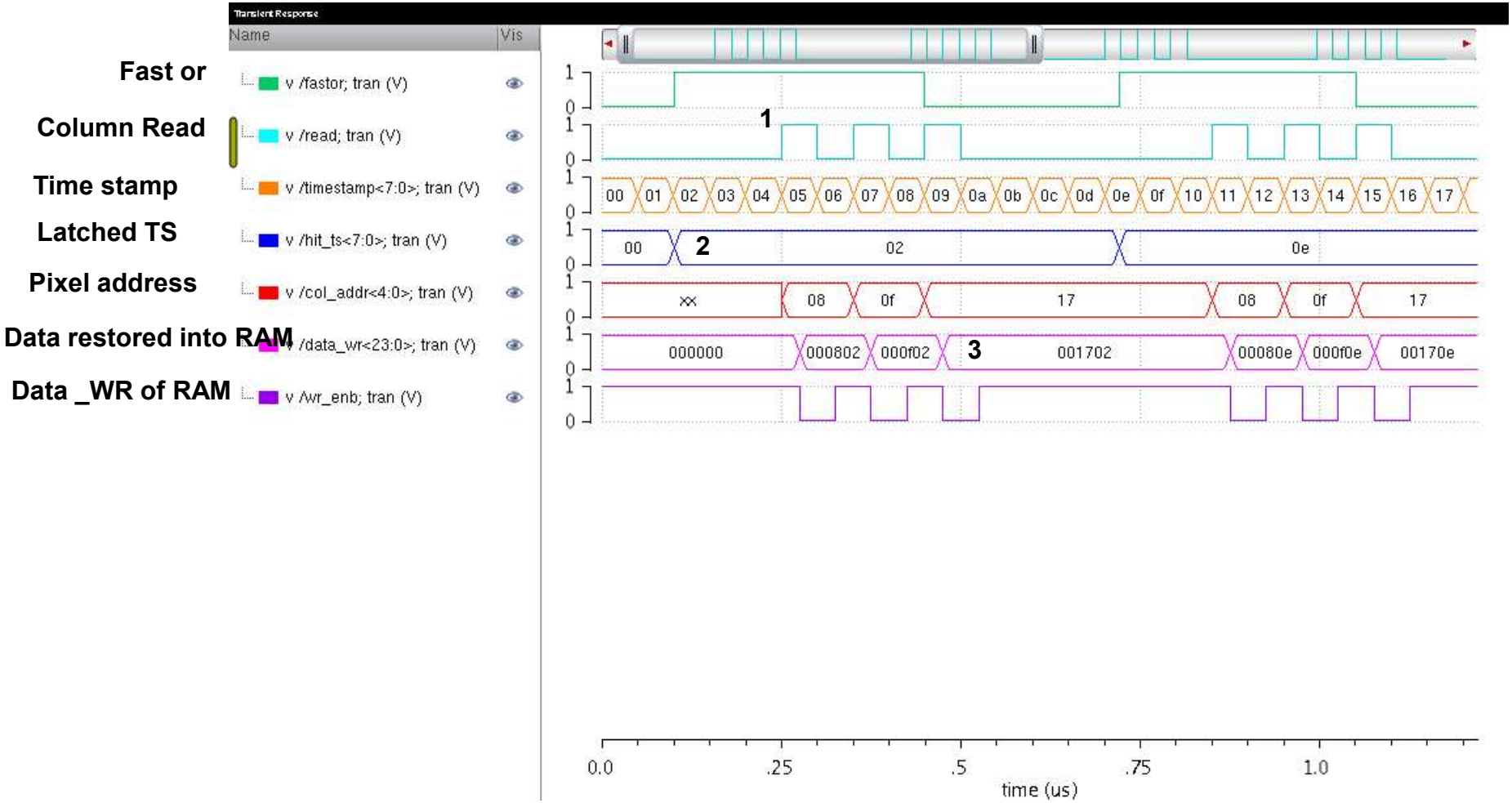
- **Similar to the ATLAS ITK readout architecture: "column-drain" readout**
  - **Priority based data driven readout**
  - **Modification: time stamp is added at EOC whenever a new fast-or busy signal is received**
  - **Dead time: 2 clk for each pixel (50ns @40MHz clk), negligible compared to the average hit rate**
- **2-level FIFO architecture**
  - **L1 FIFO: In column level, to de-randomize the injecting charge**
  - **L2 FIFO: Chip level, to match the in/out data rate between the core and interface**
- **Trigger readout**
  - **Make the data rate in a reasonable range**
  - **Data coincidence by time stamp, only the matched event will be readout**

General idea of the proposed readout architecture



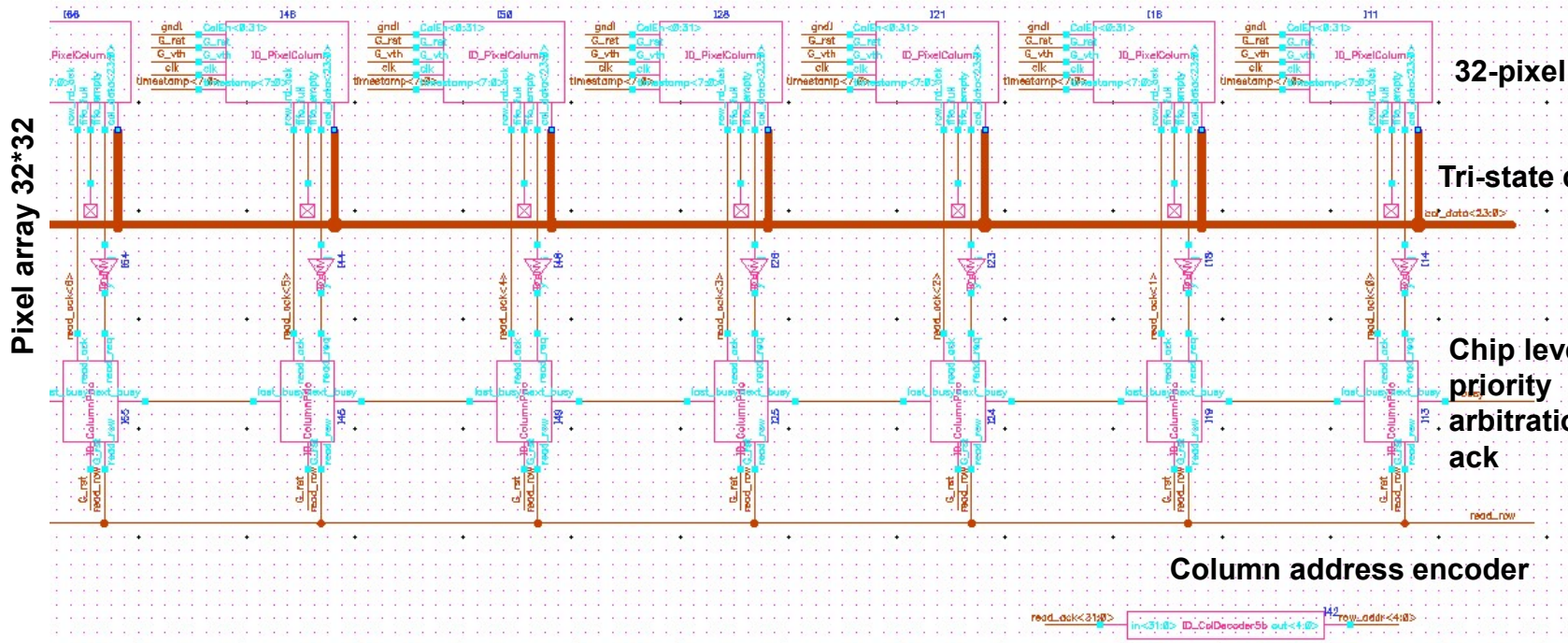
- **Readout cost: 2 clks per hit**
- **Once fast-or is clear, new hit can be accepted**
  - **A fast-or is typically for 3 pixels (1 cluster), thus dead time is typically 200ns per fast-or**
  - **Exactly the same case as in FE-I3**

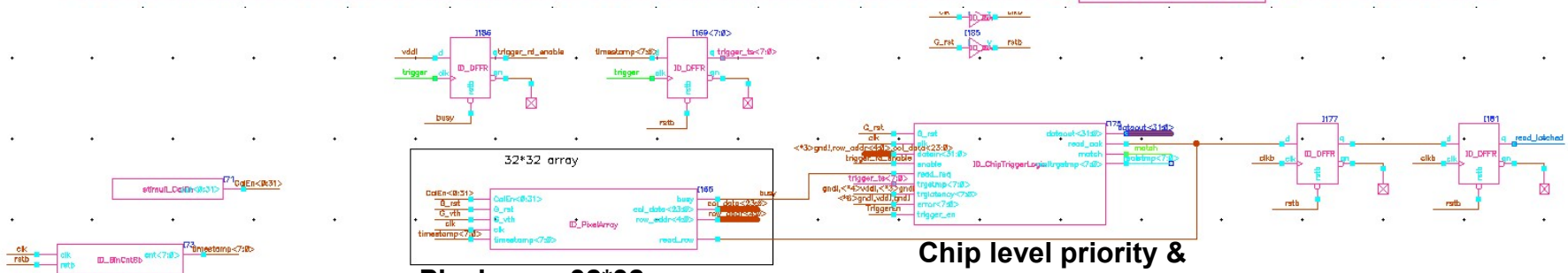
Column level simulation – behavior level



- **Pixel 08/15/23 was valid for charge injection, and was hit at the same time**
- **Can be readout sequentially by the control of priority**

Chip level logic





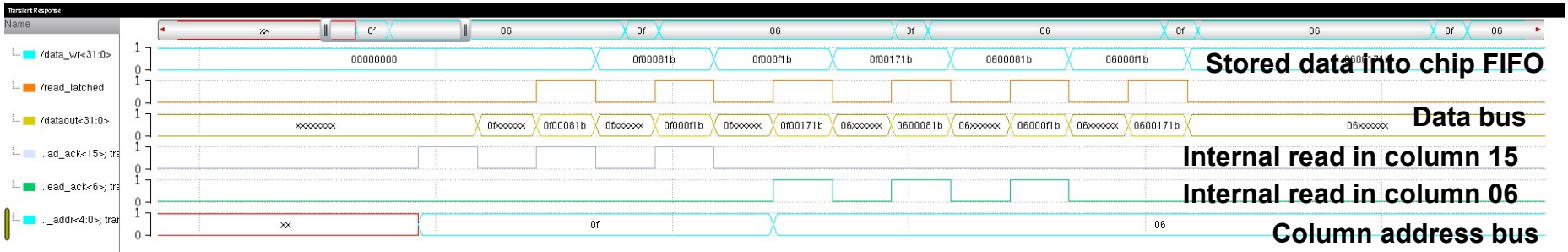
Chip level logic

- **Chip level priority**
  - **similar as the column level**
  - **Readout by the chip readout Controller**
- **Trigger logic:**
  - **Compatible with triggerless readout**
    - **Any hit will be readout under the priority arbitration**
    - **First buffered in the Chip level FIFO, then serializer (not implemented)**
  - **Trigger mode (preliminary):**
    - **Readout Controller is suspended till trigger comes**
    - **Time stamp of the trigger is latched**
    - **the time stamp of the true event is calculated, by subtracting the length of trigger latency (can be configured by the slow control)**
    - **Data readout begins, the recorded time stamp of the hits compared with the time stamp of the true event (within estimated error, can be configured by the slow control)**
    - **When matched, will be saved into the chip level FIFO, then serializer**

Chip level simulation- trigger mode

- **Column 06/15 & pixel 08/15 in each column is valid for charge injection (4 simultaneously hit pixels), with 120ns injection period, first injection@700ns**
- **Trigger comes at 4.9us, suppose trigger latency 3us, meaning the true event was at 1.9us (time stamp 4b)**
- **Simulation shows:**
  - **Trigger coincidence flag only valid during the event time stamp = 4b**
  - **Only the matched data were stored into the chip FIFO, other data streamed away**

Chip level simulation- triggerless



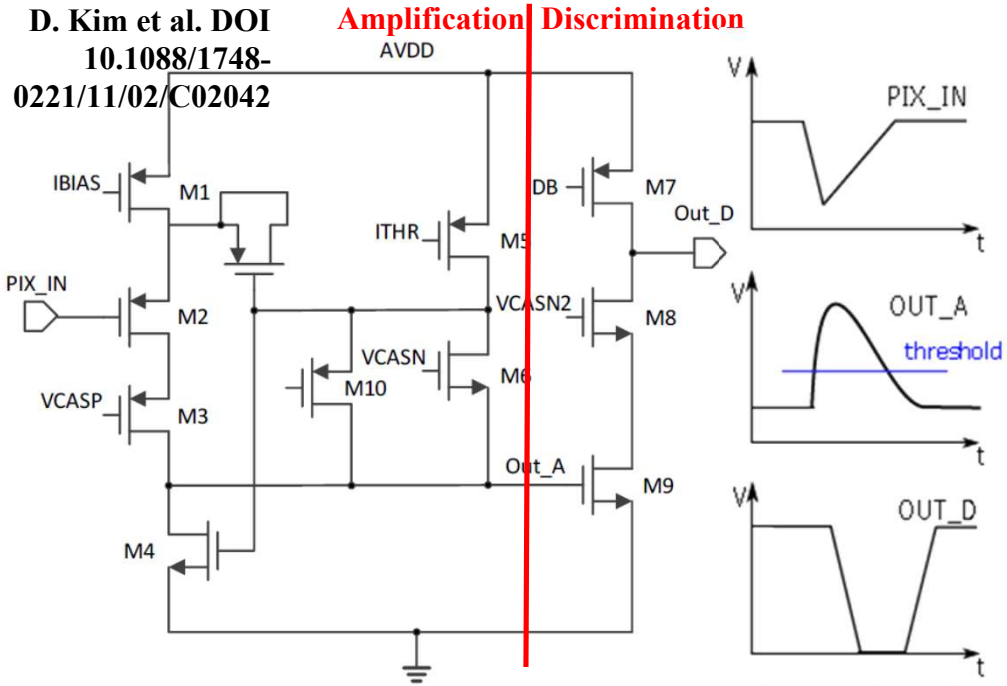
- **Column 06/15 & pixel 08/15 in each column is valid for charge injection (4 simultaneously hit pixels)**
- **Simulation shows:**
  - **Row & column address correctly encoded**
  - **Column data were readout by priority arbitration**
    - **In each column, the stored data were readout in a first-in-first-out style**
  - **Data bus can be tri-statedly loaded, while the final data that were stored into the chip FIFO is clear**

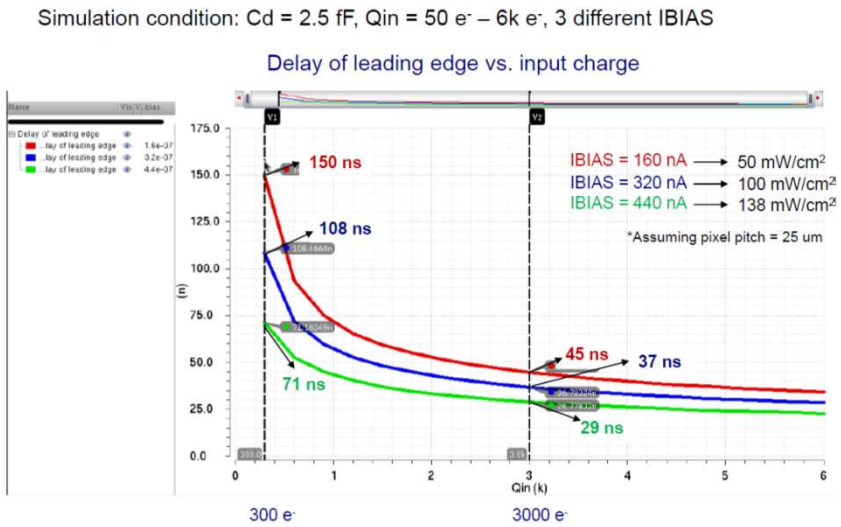
Outline

- **Specification of the CEPC Vertex Detector and Chip Design**
- **Main scheme and modification for the high-rate & fine pitch Vertex Detector**
- **Overview of the preliminary design**

Pixel architecture – Analog

D. Kim et al. DOI 10.1088/1748-0221/11/02/C02042

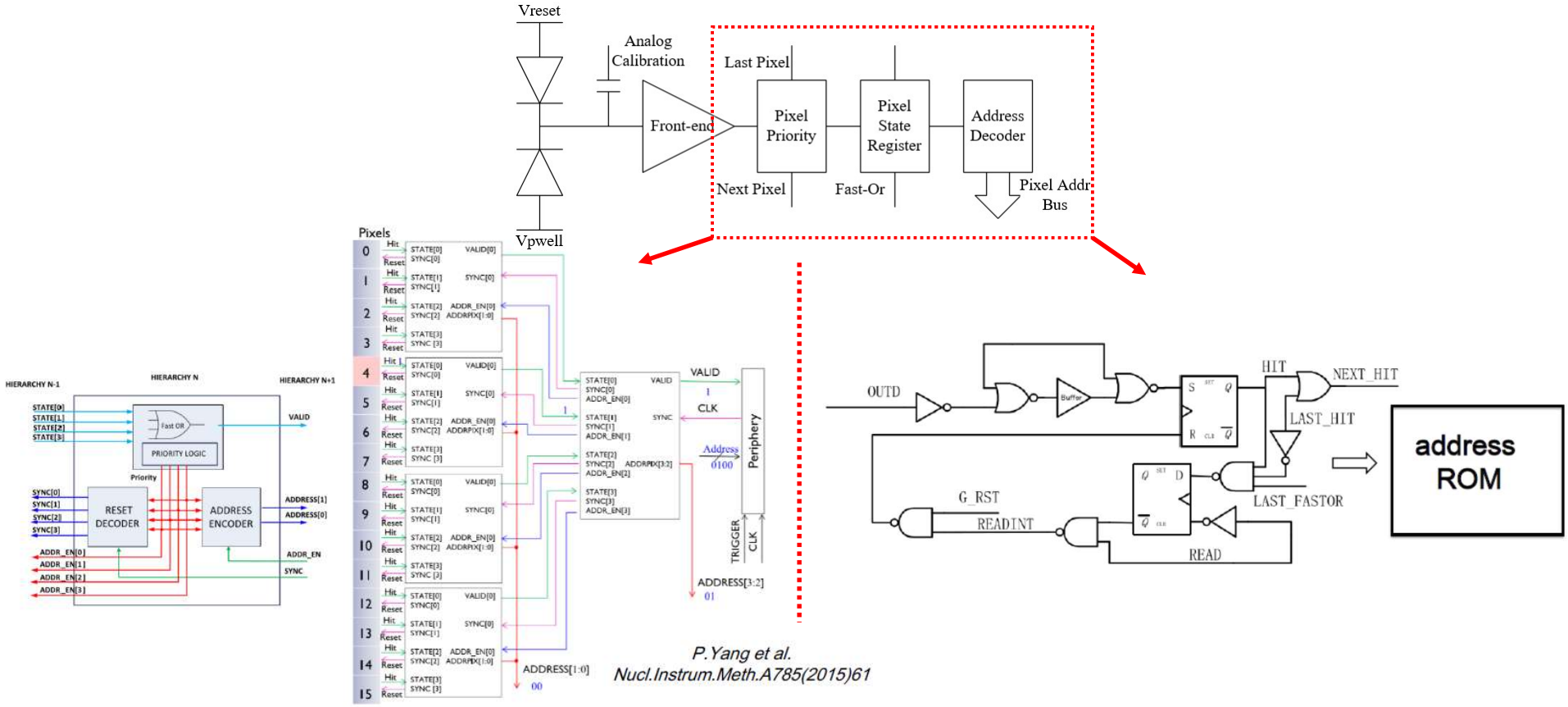




Y. Zhang for the CEPC Vertex MOST2 group meeting

- **Digital-in-Pixel scheme: in pixel discrimination & register**
- **Pixel analog is derived from ALPIDE (and benefit from MIC4 for MOST1)**
  - **As most of ATLAS-MAPS sensors' scheme**
- **Biasing current has to be increased, for a peaking time of ~25ns**
  - **Now in MOST1 ~2us peaking time was designed, too slow for 40MHz BX**
- **Consequence:**
  - **Power dissipation increased**
  - **Modified TJ process for ATLAS has to be used**
    - **With faster charge collection time, otherwise only fast electronics is of no meaning**

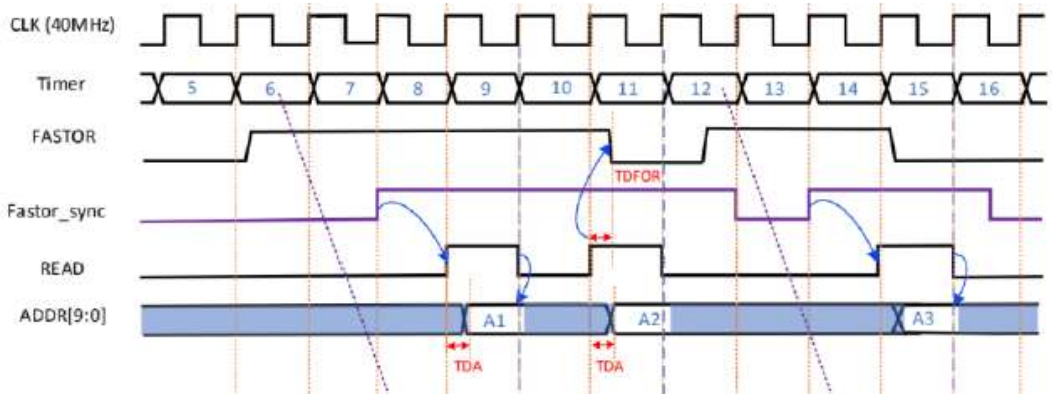
Pixel architecture – parallel digital schemes



- **Two parallel digital readout architectures were designed:**
  - **Scheme 1：ALPIDE-like: benefit from the proved digital readout in small pixel size**
  - **Scheme 2：FE-I3-like: benefit from the proved fast readout @40MHz BX (ATLAS)**

Design effort aiming for 40MHz BX on digital

- **ALPIDE-like scheme：**
  - **Fast-Or bus added to record the column hit time stamp**
  - **Boosting speed of the AERD (Address-Encoder & Reset-Decoder）**
    - **To shift the Fast-Or by a half of the clock cycle**
      - **More margin in the timing constraint of the periphery circuit**



Normal AERD

SS ; 1.6V ; 50°C	
Signal	Delay
FASTOR	14. 3ns
READ	14. 3ns
TDA	28ns
TDFOR	1. 3ns

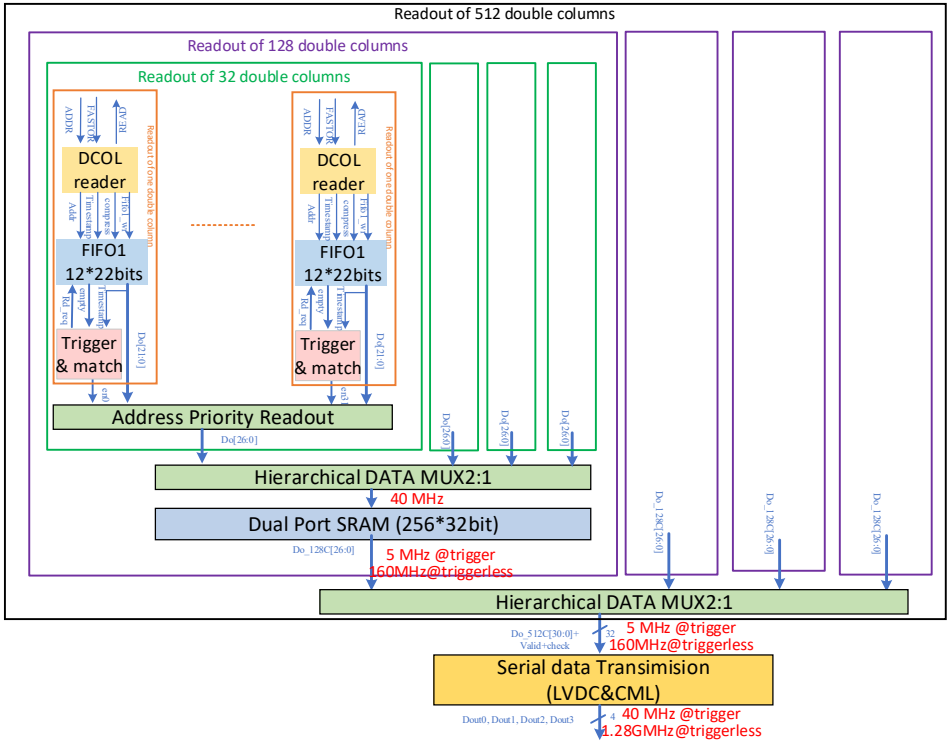
Boost AERD

SS ; 1.6V ; 50°C	
Signal	Delay
FASTOR	14. 3ns
READ	14. 3ns
TDA	25. 5ns
TDFOR	1. 3ns

TY. Wu for the CEPC Vertex MOST2 group meeting

- **FE-I3-like scheme：**
  - **Simplify the pixel cell logic**
  - **All the logic gates were re-designed with fully customized layout**
    - **For smaller pixel size**

Full chip periphery logic design



From X.M. Wei for the CEPC Vertex MOST2 group meeting

- **Main Functionality:**
  - Trigger/Triggerless readout mode compatible
    - Data coincidence and trigger window logic
  - Two level FIFOs for hit derandomization
  - High speed serialization for data readout
    - 4Gbps data rate capability

- **Other necessary blocks**
  - Slow control of the pixel array and full chip via SPI interface
  - Bias generation by current- and voltage- DACs
  - Clock management: Phase Lock Loop and serializer
  - Power management: LDOs for on-chip low ripple power supply
  - High speed interface: CML & LVDS Drivers

Team organization

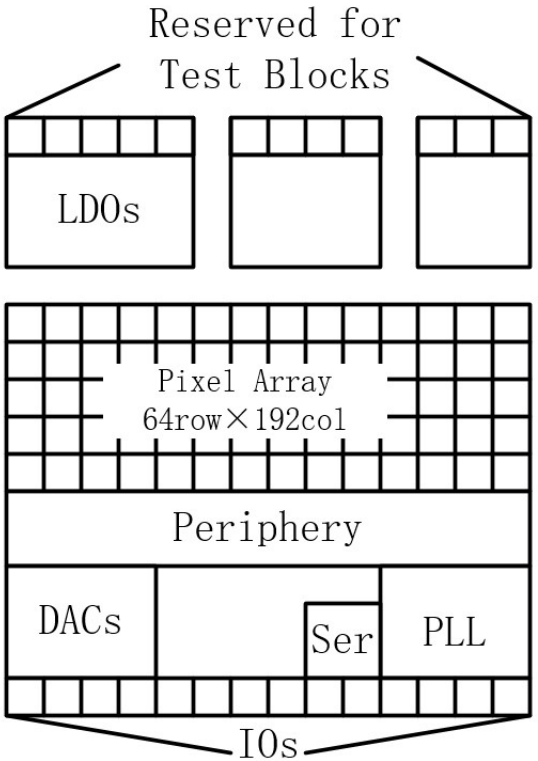
- Slides from Y. Zhang, Satellite meeting of MOST2 in Oxford, 2019.4

- **Design team:**
  - **IHEP, SDU, NWPU, IFAE & CCNU**
  - **Biweekly/weekly video design meeting on chip design (convened by IHEP)**

Institutes	Tasks	Designers
IHEP	Full chip modeling & simulation Pixel Analog, TCAD simulation High speed interface: PLL + Serializer	Wei Wei, Ying Zhang Xiaoting Li, Weiguo Lu, Mei Zhao
IFAE/CCNU	Pixel Digital	Tianya Wu, Raimon Casanova
NWPU	Periphery Logic, LDO	Xiaomin Wei, Jia Wang
SDU	Bias generation	Liang Zhang

- **Chip characterization**
  - **Test system development: SDU & + other interested parties**
  - **Electrical test: all designers supposed to be involved in the related module + other interested parties**
  - **Irradiation test: X-ray irradiator + beam line**

Current Status and recent schedule



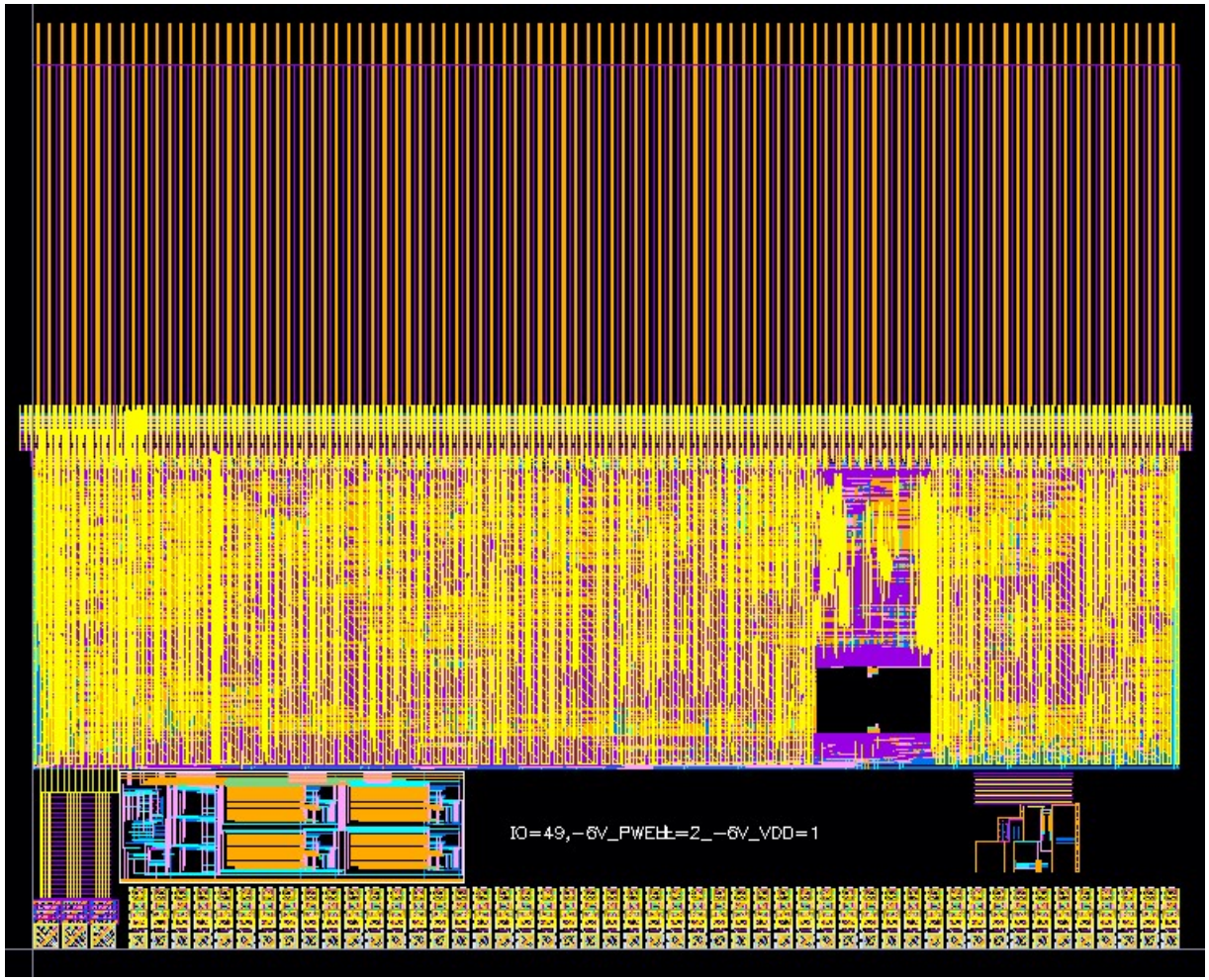
To be submitted in May

Expected to receive in Sep.

Test Board design will be in parallel

- **Design Status**
  - **Schematics of the main blocks are ready**
  - **Layout in progress**
    - **The first version of the pixel cell layout will be ready before the Mid of April**
- **First MPW tapeout**
  - **Shuttle booked for May 13th via IFAE**
    - **One block for 5mm×5mm**
  - **Organized with a full functional pixel array (small scale), plus other test blocks (less critical)**
    - **A 64×192 Pixel array + Periphery + PLL + Serializer**
    - **Bias generation included**
    - **I/O arranged in one edge, as the final chip**

Preliminary chip floorplan/layout



- **Total area: 5mm*5mm**
- **Real area: 4.8mm*3.87mm (array: 1.6mm, periphery: 1.5mm, blocks: 0.4mm, pad: 0.25mm)**

Thank you !

From vertex detector MOST1 projects towards MOST2

- **To build a prototype ladder mounted with silicon pixel sensors**
  - **Spatial resolution 3-5 μm**
  - **TID 1 Mrad**
- **Compared with MOST1 project target:**
  - **Pixel sensor prototype design**
  - **Spatial resolution 3-5 μm**
  - **Power consumption <100 mW/cm2**
  - **Integration time 100 μs**
- **MOST1 focused on key performance, however we should focus more on a full function chip that can work in a prototype system**
- **Baseline design for MOST2:**
  - **Reuse the pixel design from MOST1, with necessary modification**
  - **Focus on full chip readout architecture design, esp. fast readout and full data readout chain**

The ALPIDE readout architecture

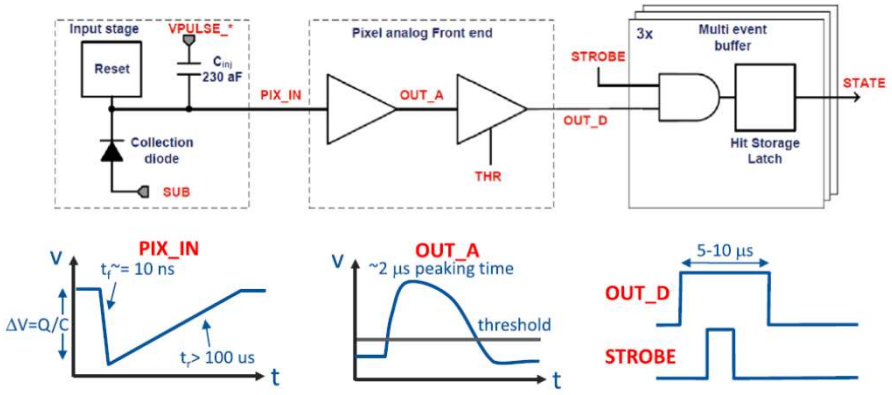


Fig. 2. Block diagram of the ALPIDE pixel cell.

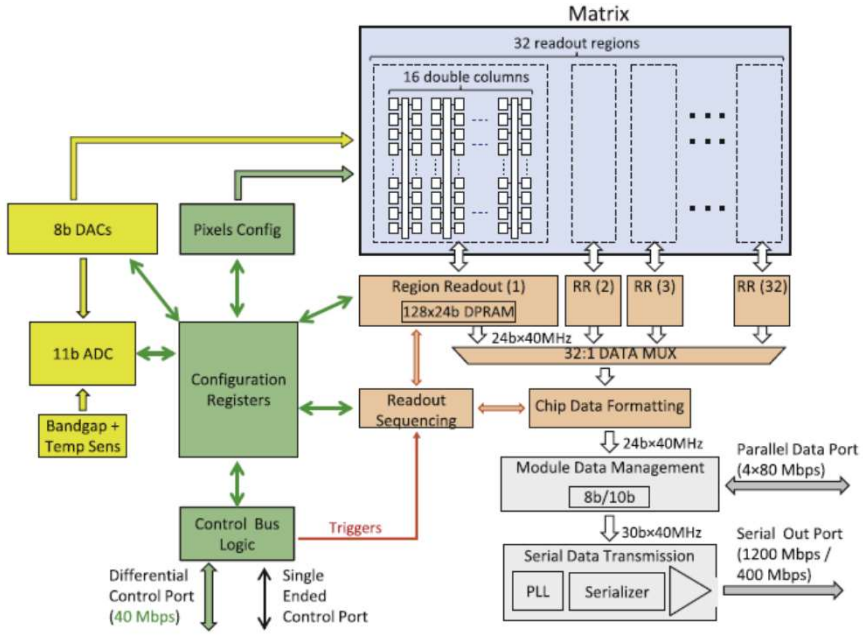


Fig. 3. Block diagram of the ALPIDE chip.

G. Aglieri Rinella et al. NIM. A 845 (2017) 583–587

Table 1
General requirements for the pixel sensor chip for the Upgrade of the ALICE Inner Tracking System. In parentheses: ALPIDE performance figure where above requirements.

Parameter	Inner barrel	Outer barrel
Chip dimensions (mm × mm)	15 × 30	
Silicon thickness (µm)	50	100
Spatial resolution (µm)	5	10 (5)
Detection efficiency	>99%	
Fake hit probability (evt^{-1} $pixel^{-1}$)	$<10^{-5}$ ($<< 10^{-5}$)	
Integration time (µs)	<30(10)	
Power density (mW/cm^2)	<300(~ 35)	<100(~ 20)
TID radiation hardness[a] (krad)	2700	100
NIEL radiation hardness[a] (1 MeV n_{eq}/cm^2)	1.7×10^{13}	1×10^{12}
Readout rate, Pb–Pb interactions (kHz)	100	

[a] 10 × the radiation load integrated over the approved program (6 years of operation).

- **The ALPIDE architecture, as MOST1 referenced, uses strobe signal as the "trigger"**
- **However, the readout rate is only ~100kHz, and more like frame readout**

Discussion on ALPIDE – analysis & conclusion

- **Architecture of the pixel analog has to be modified, if trigger logic has to be used**
  - **Time stamp can only be added at the EOC, due to limited pixel size**
  - **Thus hit info has to be sent immediately to the EOC (A fast-or-like signal), while pixels waiting for readout (and reset)**
    - **Not possible for the current ALPIDE pixel analog**
    - **Modification should be done to generate the "fast-or"**
  - **CEPC: trigger rate is much less than hit rate**
    - **Meaning pixel has to be readout and reset asap, not waiting for trigger**
      - **Meaning frame-like readout is not possible**
- **ALPIDE Periphery logic almost compatible with CEPC**
  - **Priority Encoder@double column level, and de-randomizing memories are the common scheme in similar chips**
  - **However, trigger matching logic should be added if expecting output data rate at reasonable level**

Discussion on ALPIDE – analysis & conclusion

- **ALPIDE is not fully compatible with CEPC vertex & other high hit rate, high bunch crossing applications (like ATLAS)**

1. **Bunch crossing too high**
   - **Now bunch crossing at 100~200kHz (i.g. frame rate)**
   - **While CEPC 1.5MHz (Higgs) ~ 40MHz(Z pole)**
     - **Not possible for the chip level frame-like readout, because:**
       - **At least 120MHz clk has to run at periphery-column level (3pixel per hit)**
       - **ALPIDE is "triggerless", no further data reduction, data rate too high (*32bits per hit)**
2. **Pixel analog should be (much) faster**
   - **now 2us peaking, 10us duration**
   - **CEPC: "Hit rate: 120MHz/chip, or 225Hz/pixel (average), 120kHz/col (ave)", Meaning every 8.3us, the column will be hit, however, very unlikely to be at the same pixel**
   - **For CEPC, peaking time should be much faster (25ns level)**
     - **Otherwise leads to too large delay for the arrival time stamp (although can be covered by the configurable trigger match error)**
   - **For CEPC, duration should also be faster**
     - **Better ends earlier than 8.3us, avoiding continuous hit in the same pixel**
   - **Larger power expected than ALPIDE**

Further analysis for the proposed readout

Average hit rate with <1% data loss	400	MHz/cm^2	3.2µs trigger latency, 100KHz trigger rate.
Readout initiation	Trigger		
Max. number of consecutive triggers	16		
Trigger latency (max)	6.4	µs	
Maximum sustained trigger	200	KHz	
External clock input	40	MHz	
Serial command input	40	Mb/s	1 input for chip
Serial data output	160	Mb/s	1 output for chip
Output data encoding	8b/10b		
I/O signals	~LVDS		Current balanced differential

- **Readout scheme similar like FE-I3, which is for ATLAS**
- **CEPC is of much less hit rate than ATLAS, while the BX clk is the same**
  - **ATLAS: 400MHz/cm^2 hit rate, CEPC: ~36MHz/cm^2**
  - **ATLAS: Trigger latency 3.2us, suppose CEPC is the same**
  - **ATLAS: 100kHz trigger rate, suppose CEPC is the same or less**
- **Since FE-I3 fit well for the ATLAS requirement, the proposed readout architecture should work for CEPC**
- **How the pixels were grouped (as discussed in many CMOS sensors) was not shown in the behavior level model, but it doesn't affect the detecting ability**
  - **The main purpose of grouping is optimization: e.g., address routing, power dissipation**