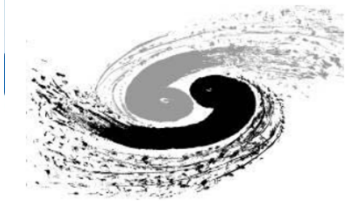



Design of on-chip LDO for CMOS pixel sensor

Jia Wang

School of computer science

Northwestern Polytechnical University

2019.4.30

Outline

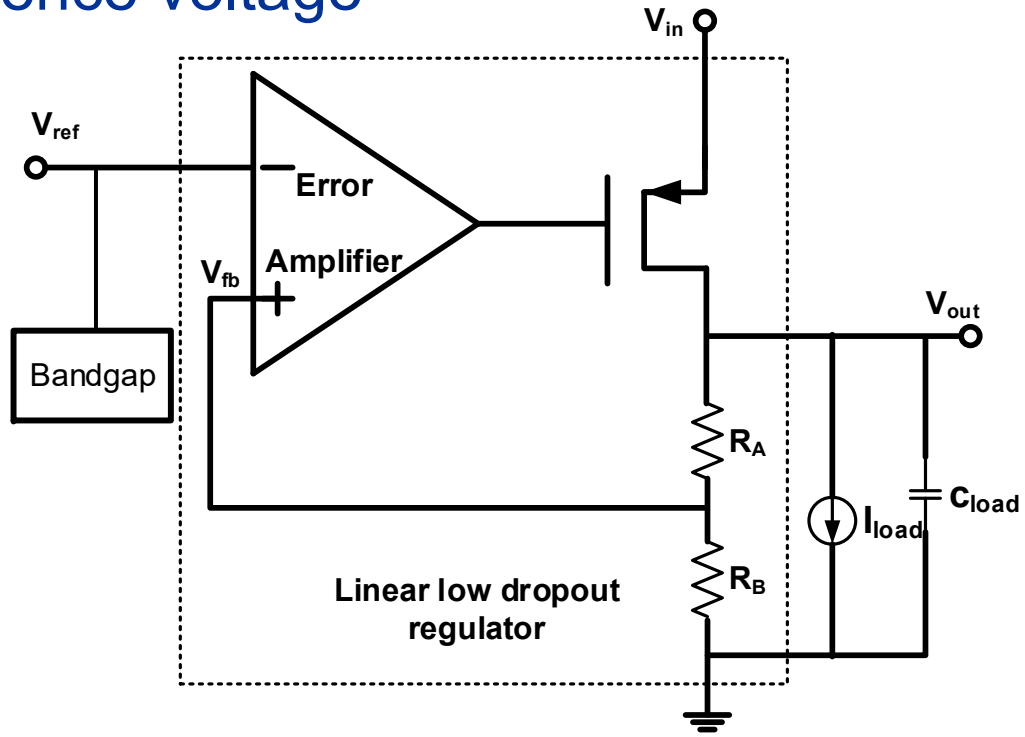
- Design requirement
- Circuit design
  - Bandgap
  - LDO
- Summary

Design requirement

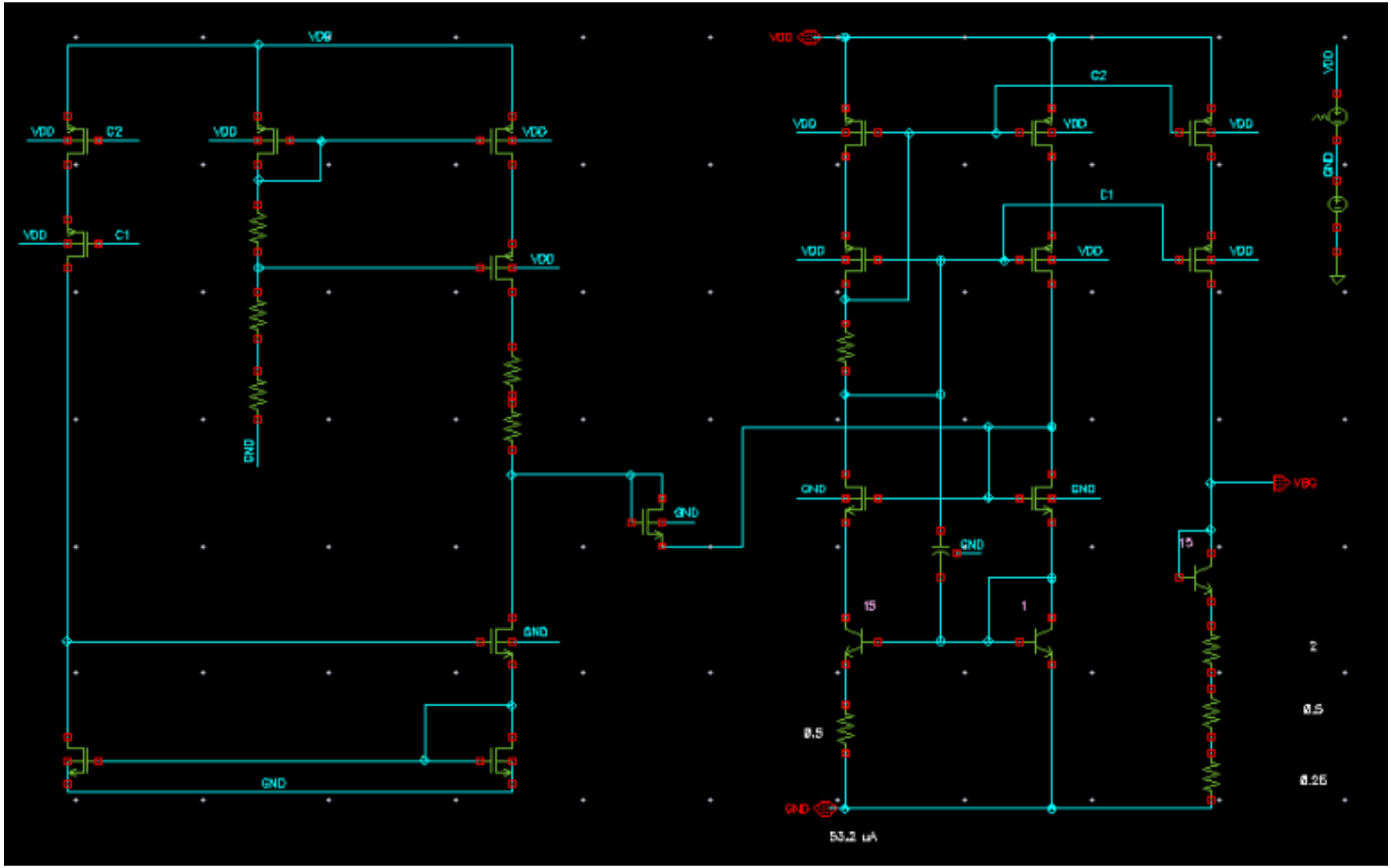
Parameters	Value
Input voltage	<2 V
Output voltage	1.8 V
Maximum output current	200 mA
Load capacitance	~200 nF
TID	> 1 Mrad.
Maximum dropout voltage	0.2 V
Fully integrated on-chip	
Low noise, High PSR	

Circuit design

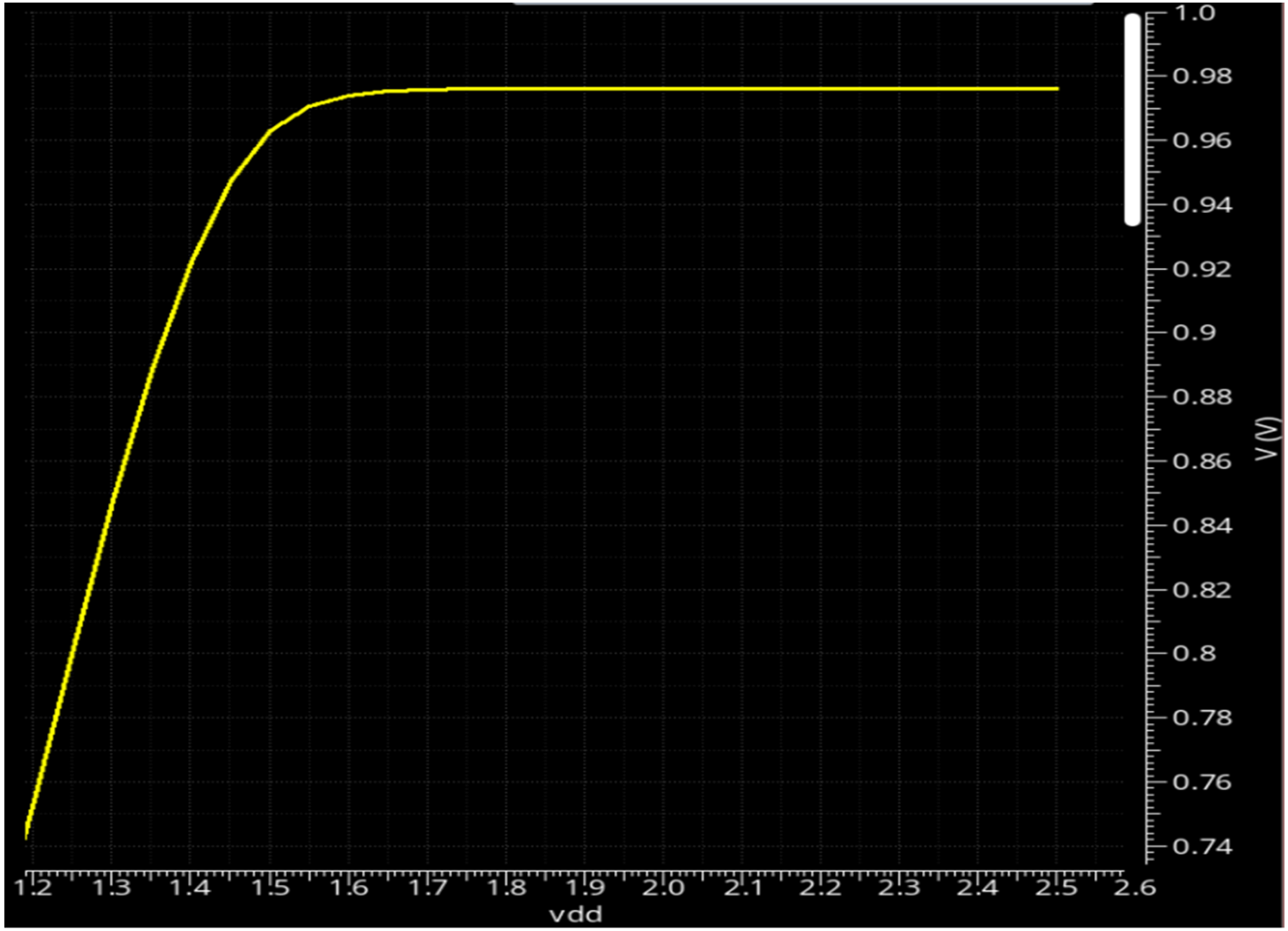
- Two blocks
  - Bandgap
    - supplying reference voltage
  - LDO



Schematic of Bandgap

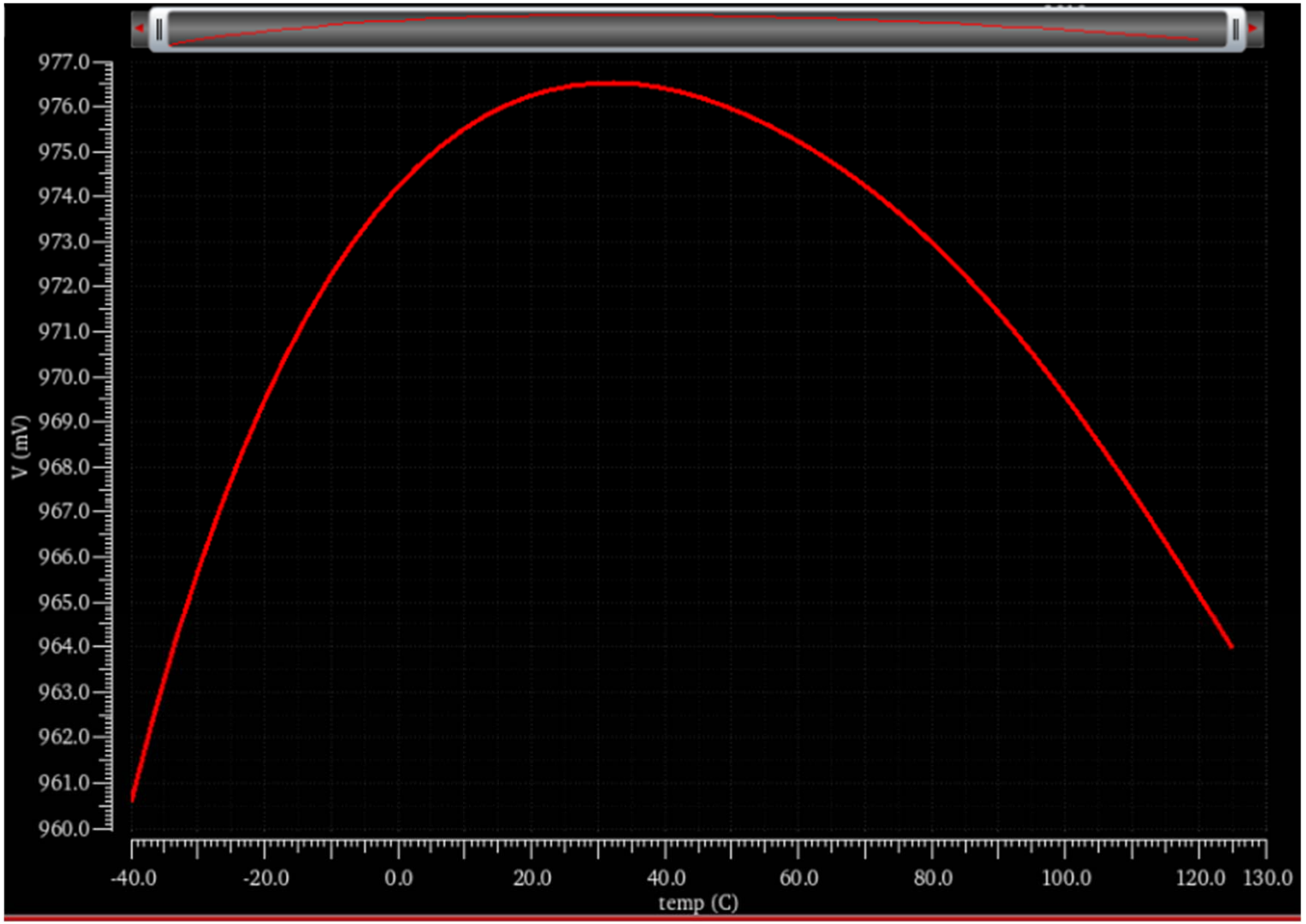


Simulation Results

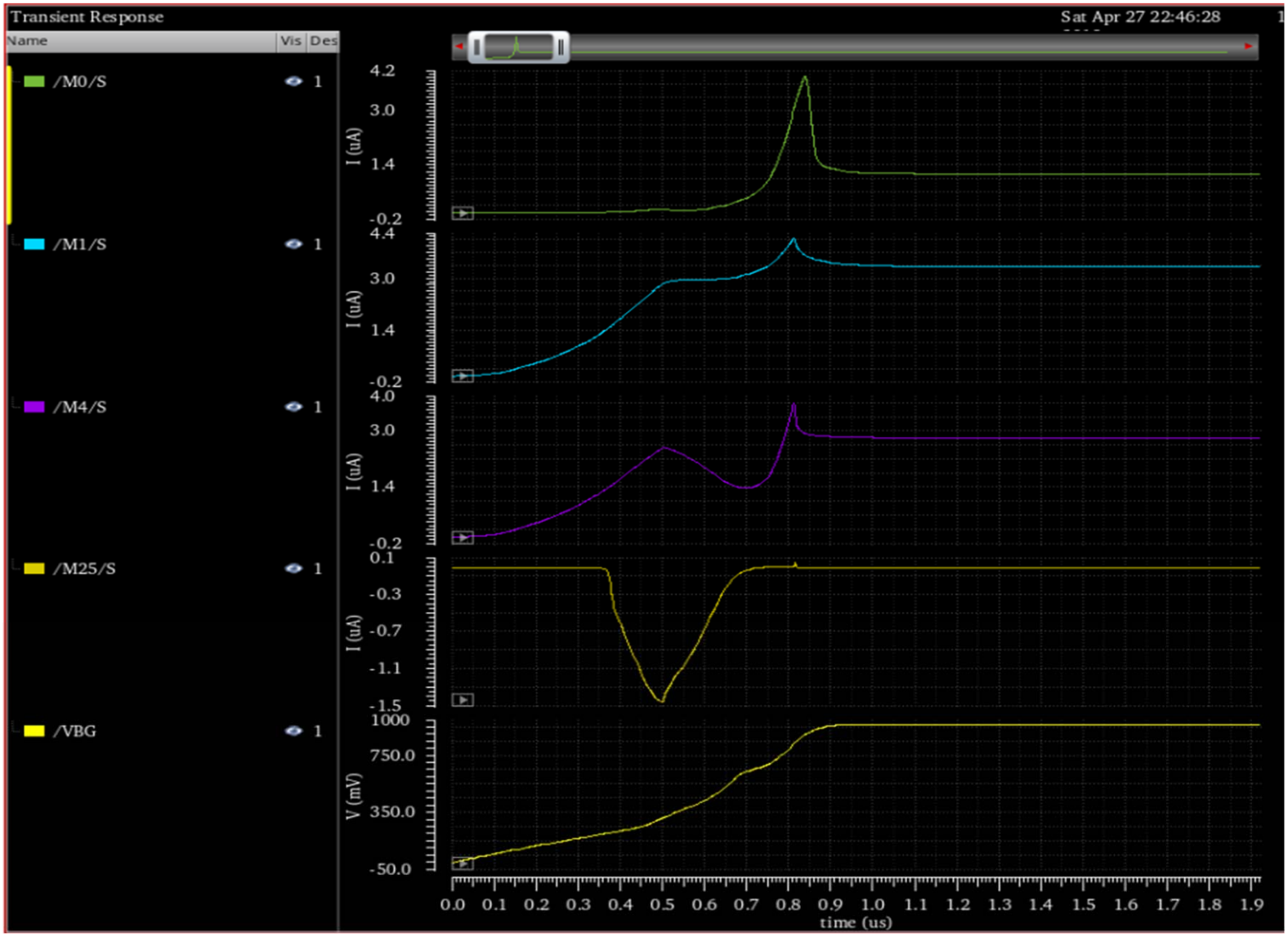


Vbg=0.976 V @ Vdd ≥ 1.8 V

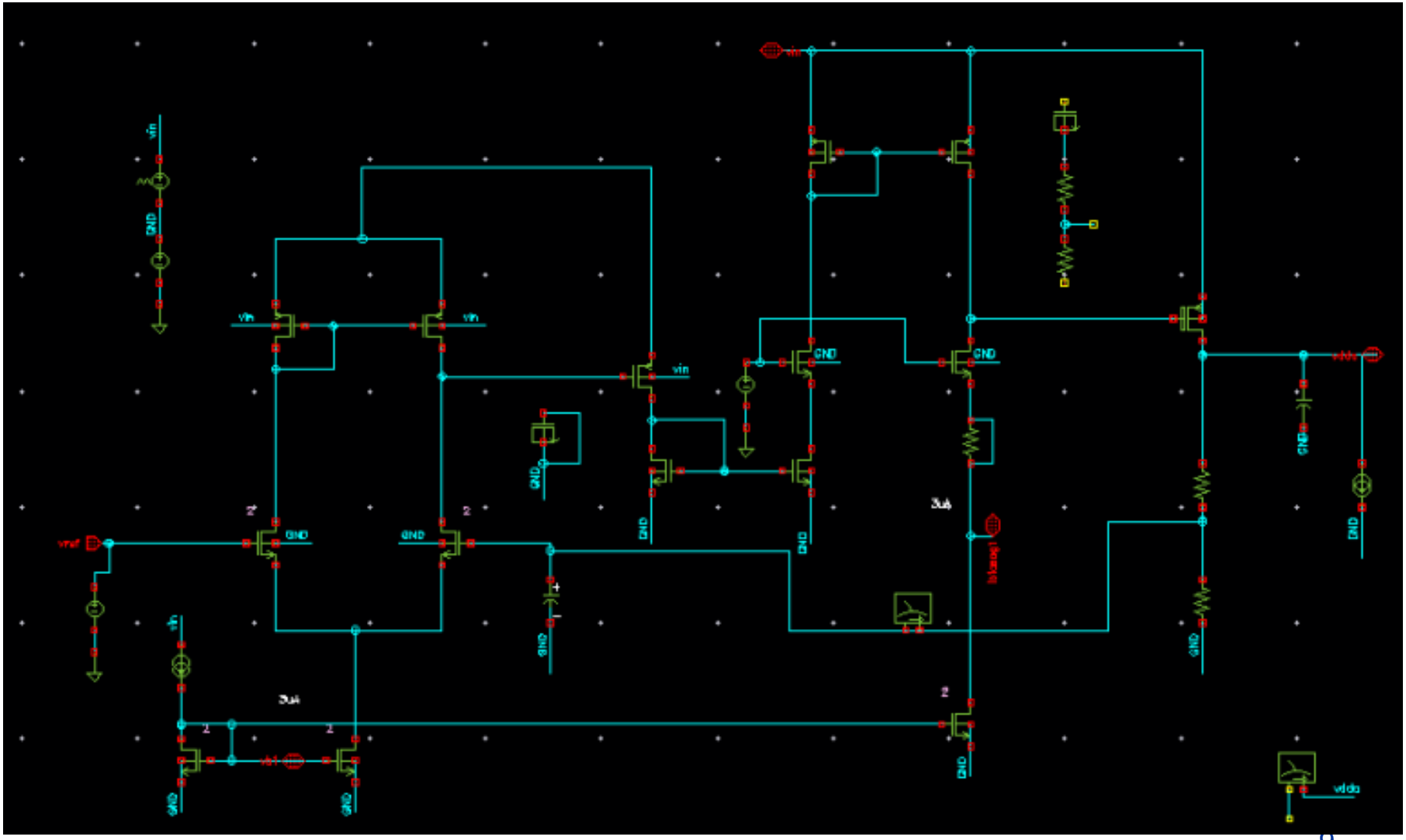
VBG VS Temperature



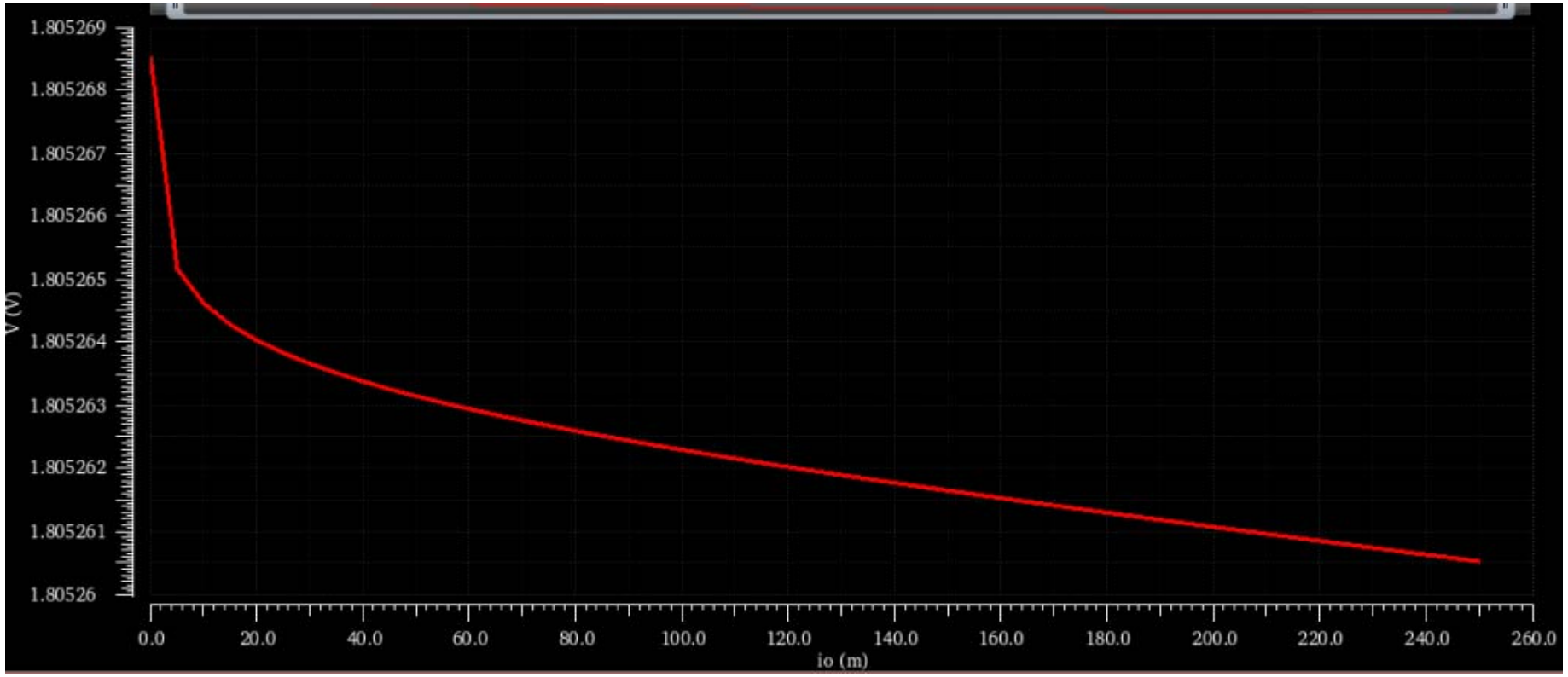
Start-up


Transient Response
Sat Apr 27 22:46:28
Name
Vis
Des
/M0/S
/M1/S
/M4/S
/M25/S
/VBG
I (uA)
V (mV)
time (us)

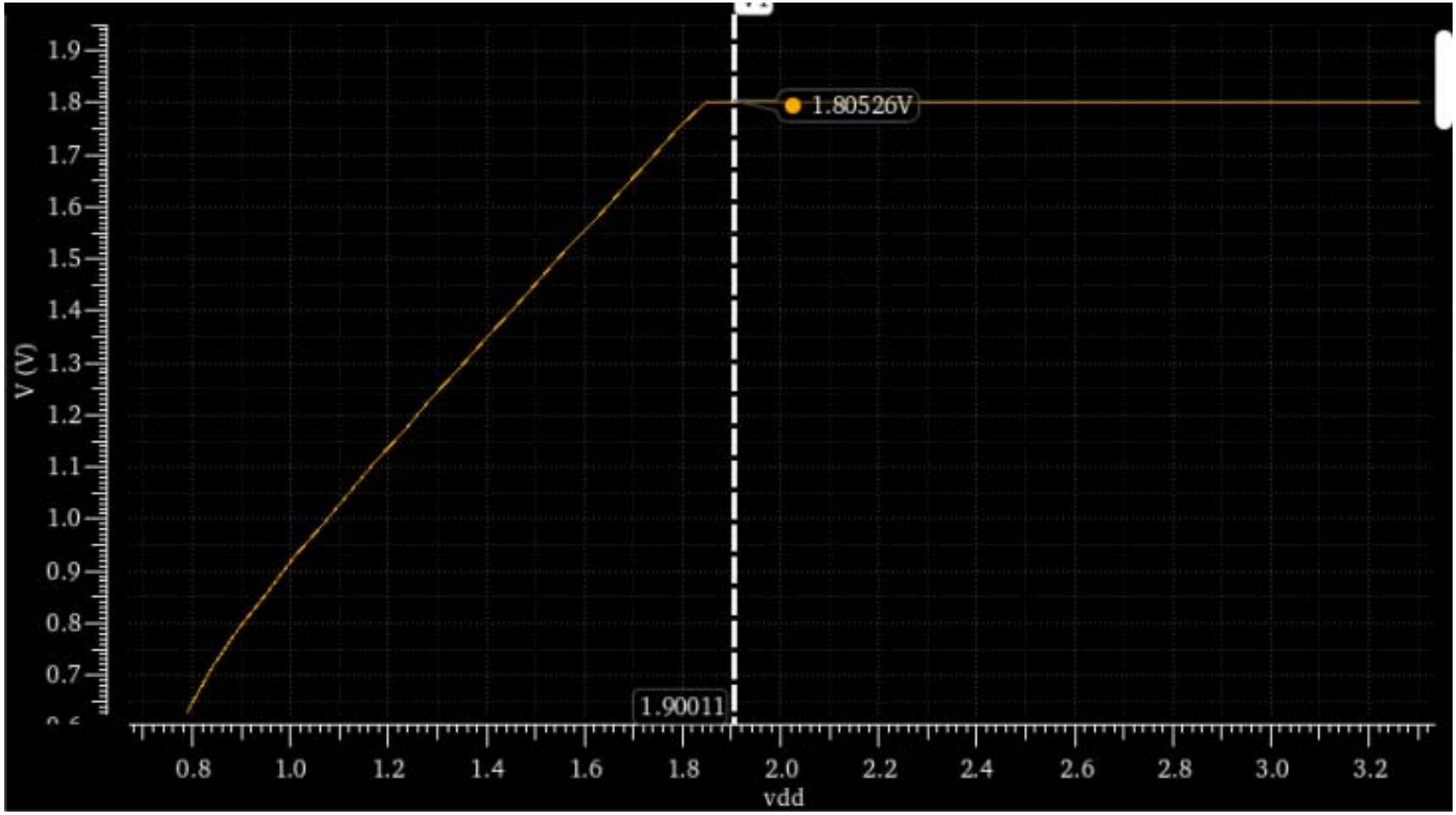
LDO



V_{out} VS I_{load} @ V_{in}=2 V



V_{in} VS V_{out} @ I_{load}=0.2A



Summary and next work

- Bandgap circuit design has been finished.
- LDO circuit design is under going.
- Layout will be finished in 7 days.
- IO PAD？
- 1.8 V or 3.3 V MOS？