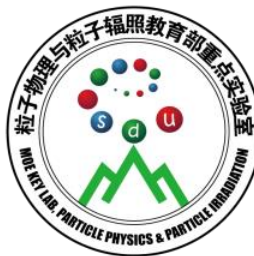




山东大学
SHANDONG UNIVERSITY



粒子物理与粒子辐照
教育部重点实验室

Current DAC & Voltage DAC

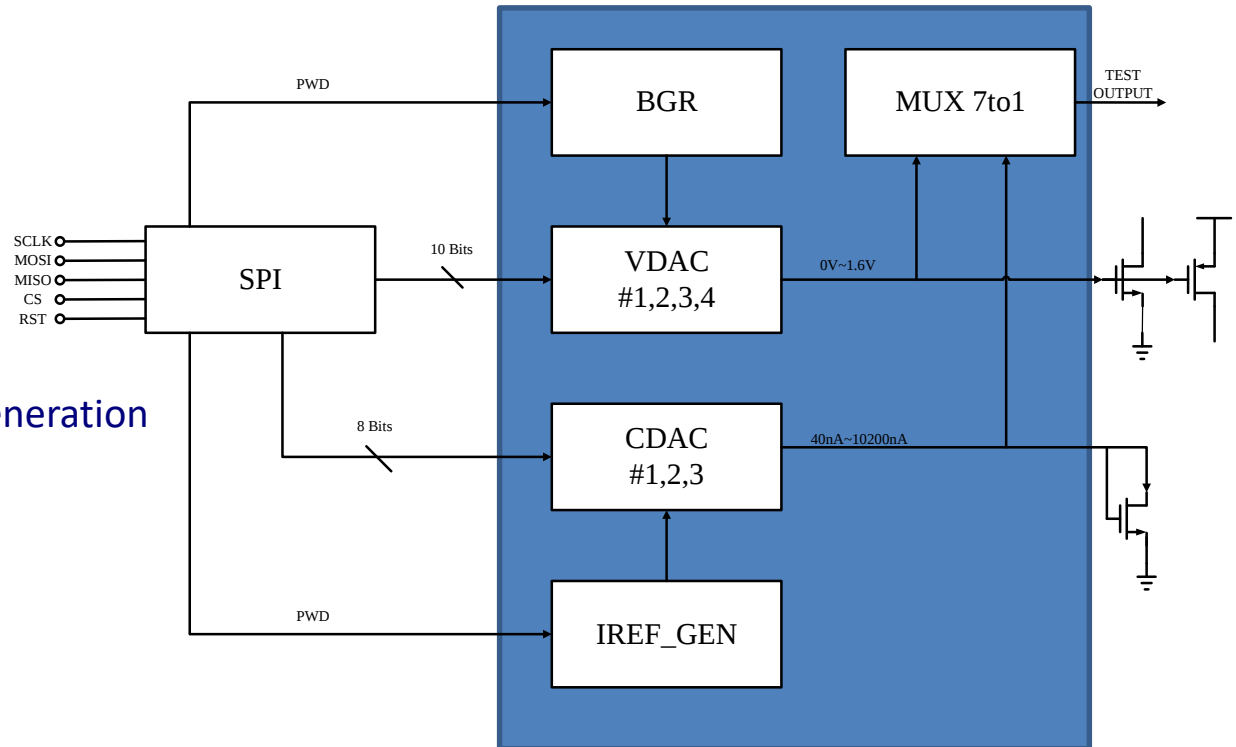
Liang Zhang

2019-4-30

Structure of DAC

■ Structure of the DAC

- Voltage DAC (VDAC)
- Current DAC (CDAC)
- Bandgap(BGR)
- MUX 7to1
- Current bias reference generation



Architecture of the top DAC

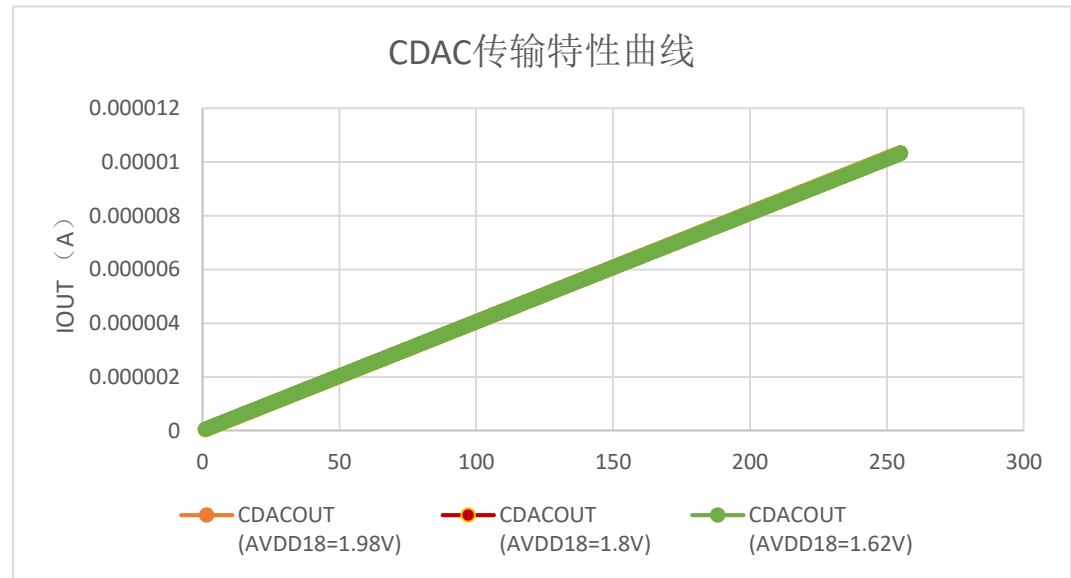
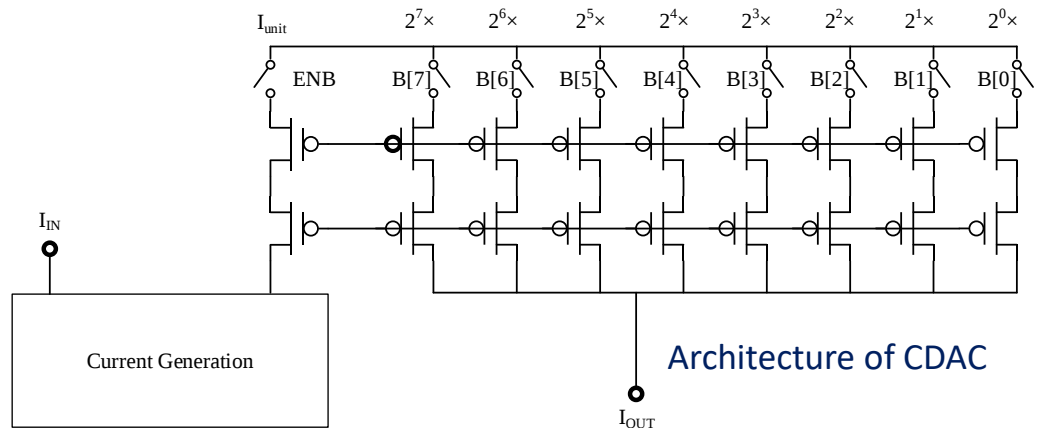
■ Characteristics

- Voltage DAC (VDAC)
 - 10 bit
 - LSB: 1.56 mV
 - Range: 0 – 1.6 V
- Current DAC (CDAC)
 - 8 bit
 - LSB: 40 nA
 - Range: 0 nA ~ 10.2 μ A

Structure of current DAC (CDAC)

■ Current DAC

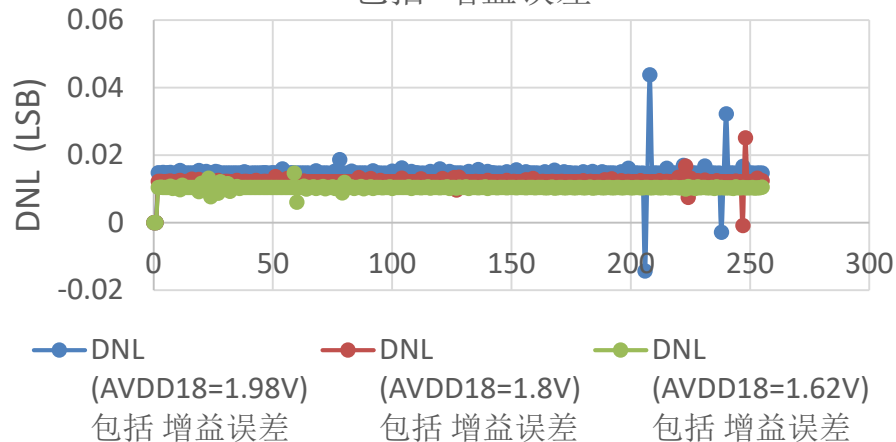
- ↗ Current mirror
- ↗ Segmented architecture
 - 4 most significant bits (MSB)
 - ★ thermometer decode
 - 4 least significant bits (LSB)
 - ★ binary weighted
- ↗ Output impedance
 - Min: 104K Ω
 - Max: 43 M Ω



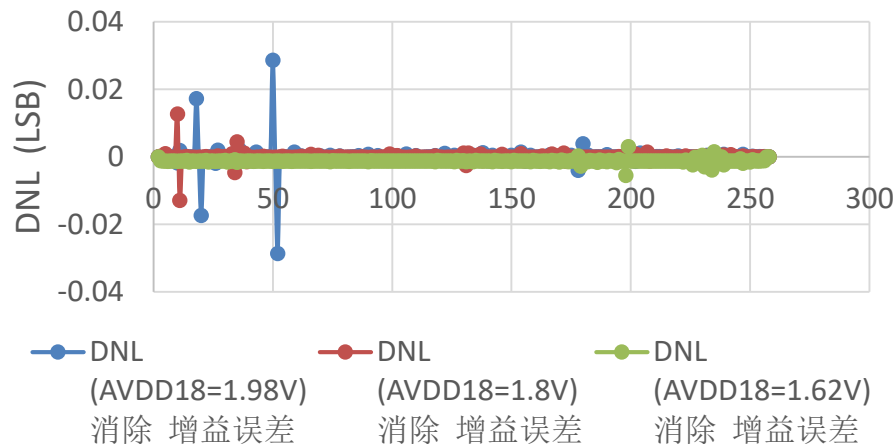
Characteristic curve of the CDAC

Simulation results of current DAC (CDAC)

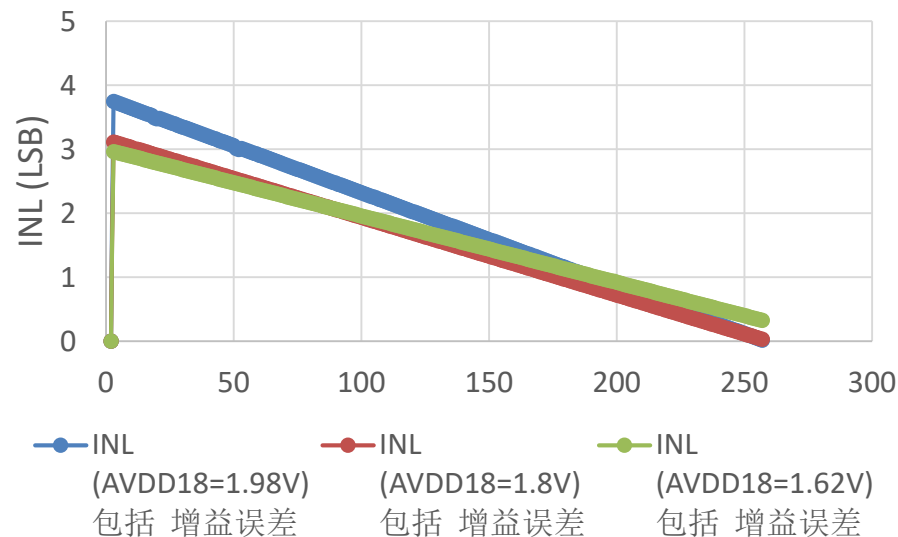
DNL曲线
包括 增益误差



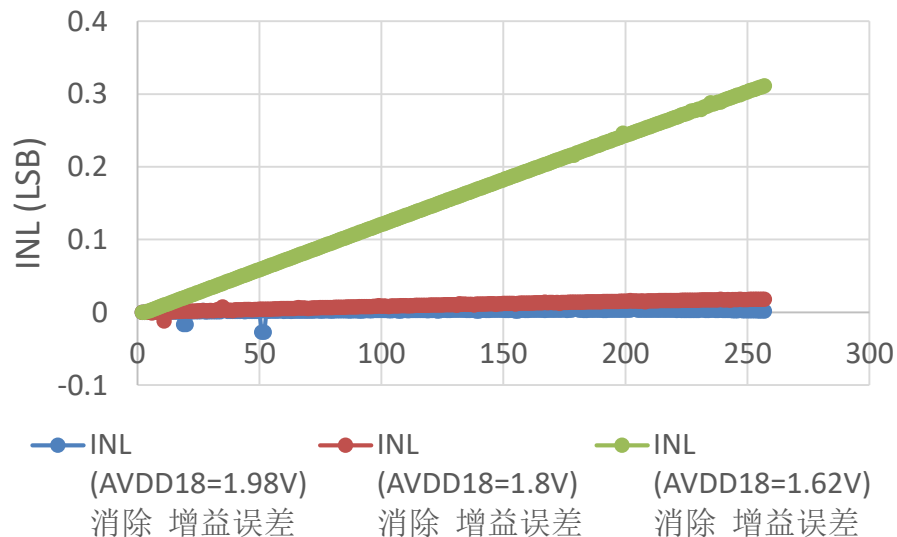
DNL 曲线
消除 增益误差



INL 曲线 包括增益误差



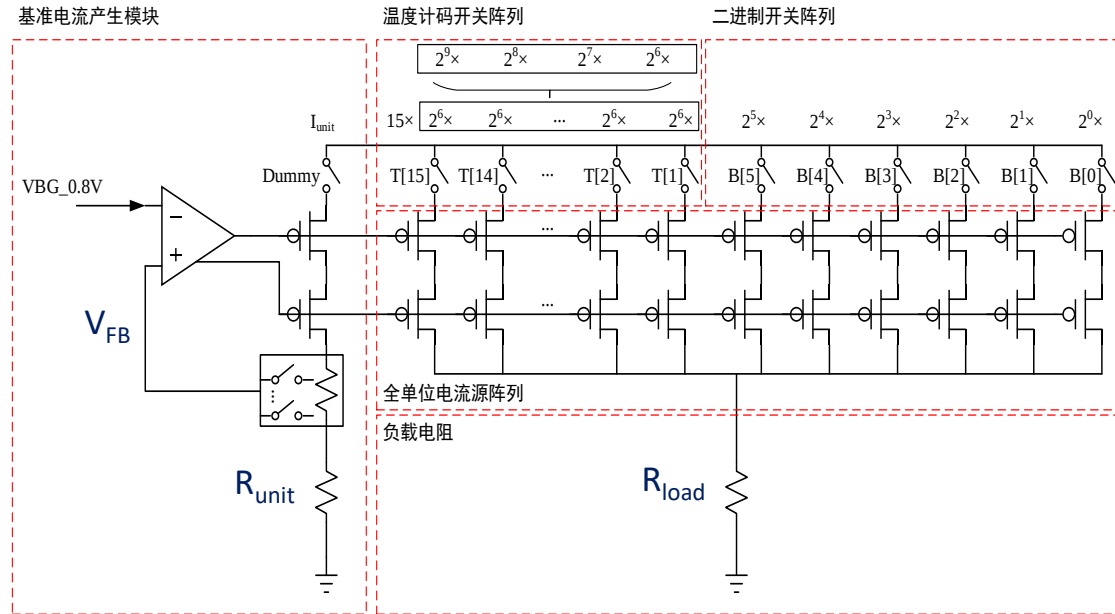
INL 曲线 消除增益误差



Structure of voltage DAC (VDAC)

■ Voltage DAC

- ⇒ Current bias generation block
 - VBG: output of bandgap ~ 0.8 V
 - $I_{unit} \sim 20 \mu A$
- ⇒ Negative feedback to stabilize VBG @ 0.8 V
- ⇒ Current mirror with resistor load
- ⇒ Segmented architecture
 - 4 most significant bits (MSB): thermometer decode
 - 6 least significant bits (LSB): binary weighted

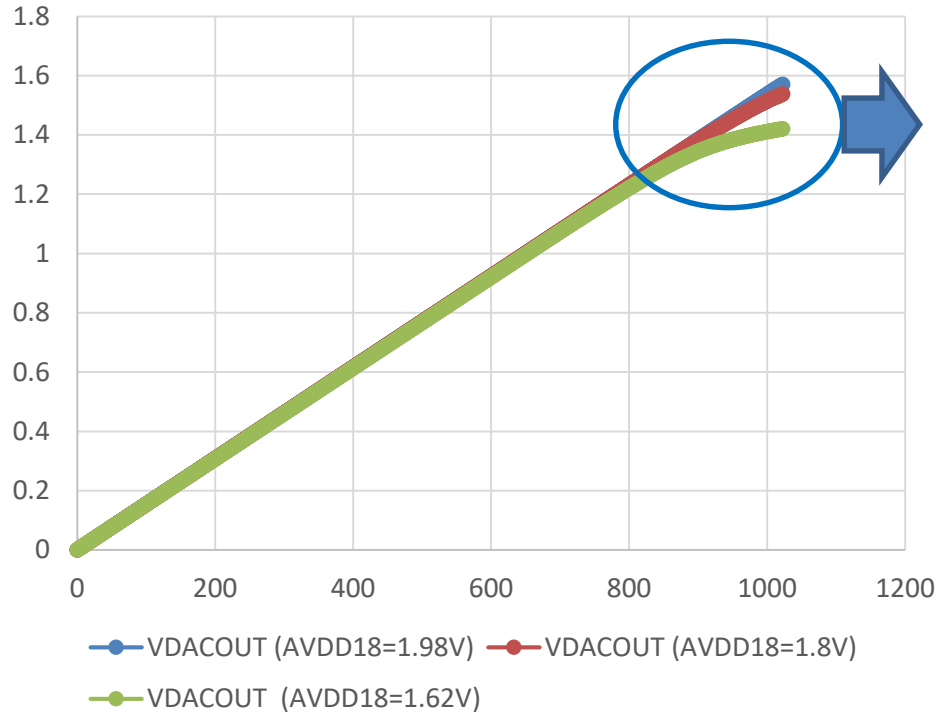


Architecture of CDAC

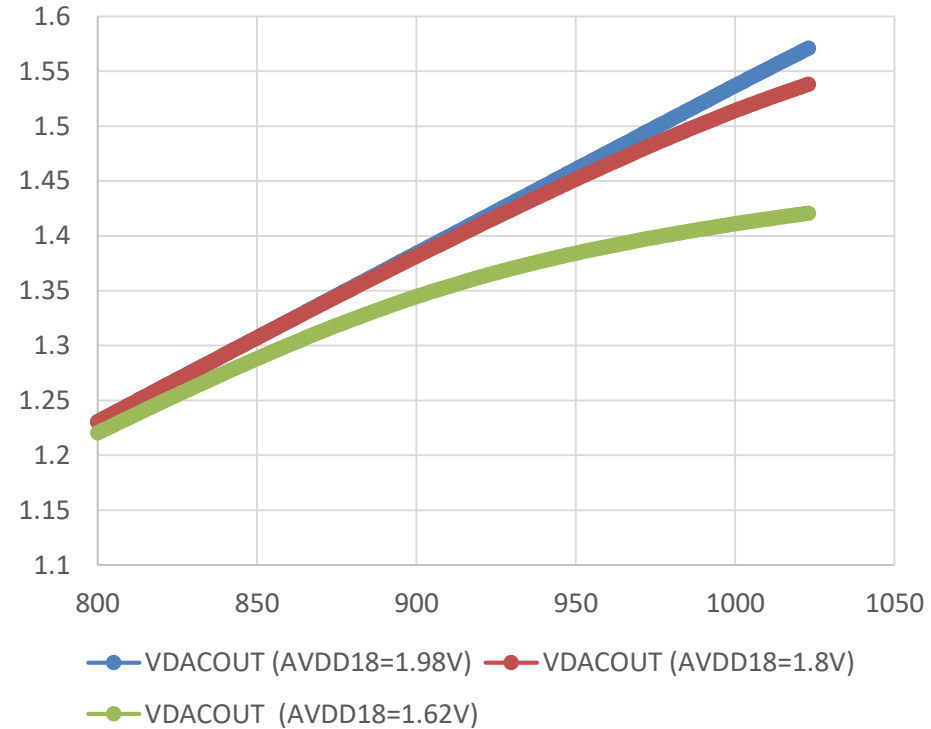
$$\begin{aligned}
 V_{DAC} &= Weight(Code[9:0]) \times I_{unit,mirror} \times R_{load} \\
 &= Weight(Code[9:0]) \times \left(\frac{1}{4} \times I_{unit,ref} \times \frac{1}{4} \times R_{unit} \right) \\
 &= \sum_{i=0}^9 2^i \cdot Code[i] \times \left(\frac{1}{4} \times I_{unit,ref} \times \frac{1}{4} \times R_{unit} \right) \\
 &= \sum_{i=0}^9 2^i \cdot Code[i] \times \frac{1}{512} \times V_{FB} \\
 &= \sum_{i=0}^9 2^i \cdot Code[i] \times V_{LSB}
 \end{aligned}$$

Structure of voltage DAC (VDAC)

VDAC传输特性曲线

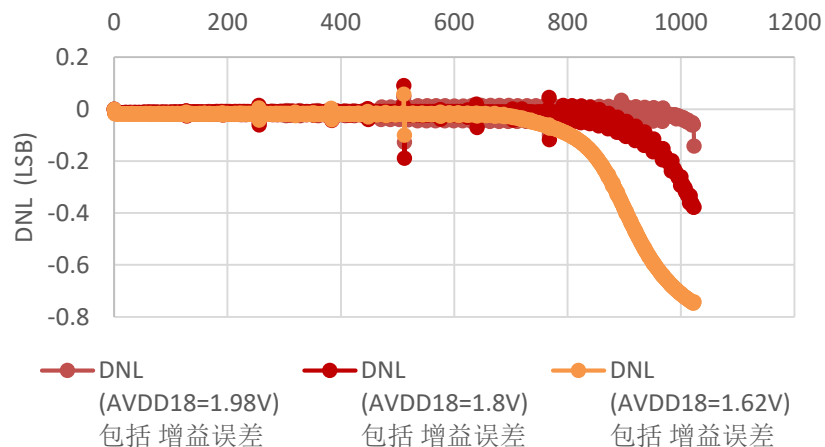


VDAC传输特性曲线

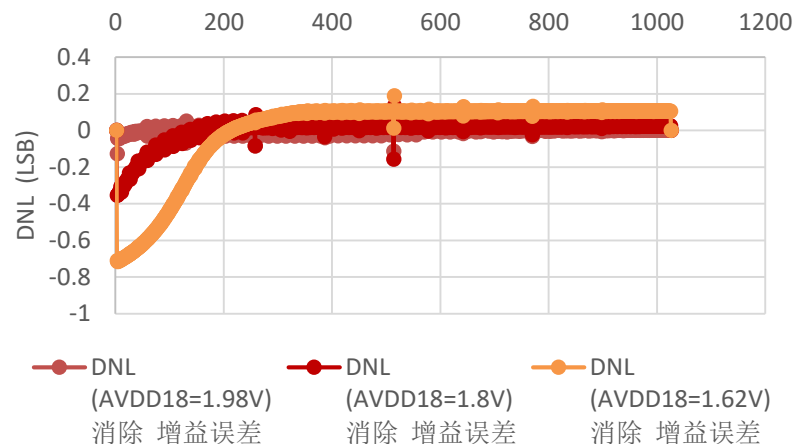


Simulation results of voltage DAC (VDAC)

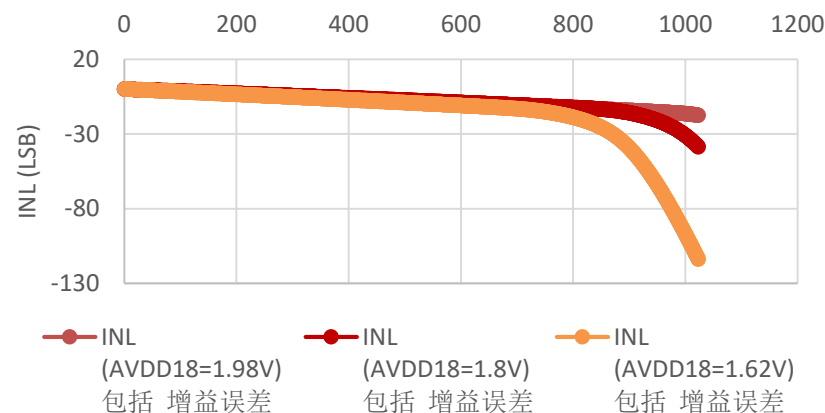
DNL曲线 包括增益误差



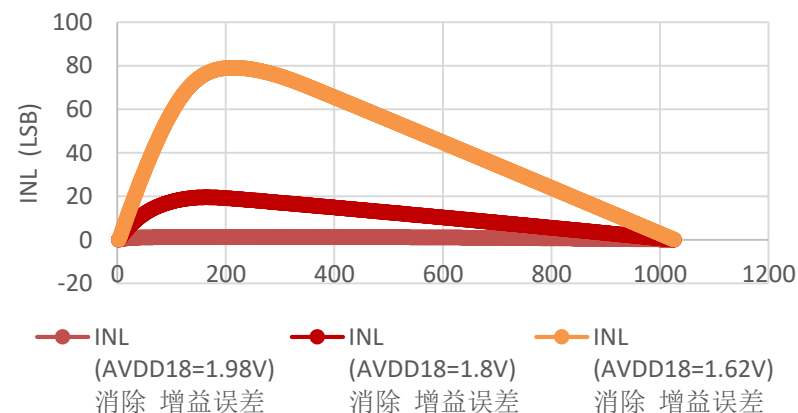
DNL 曲线 消除增益误差



INL误差 包括增益误差

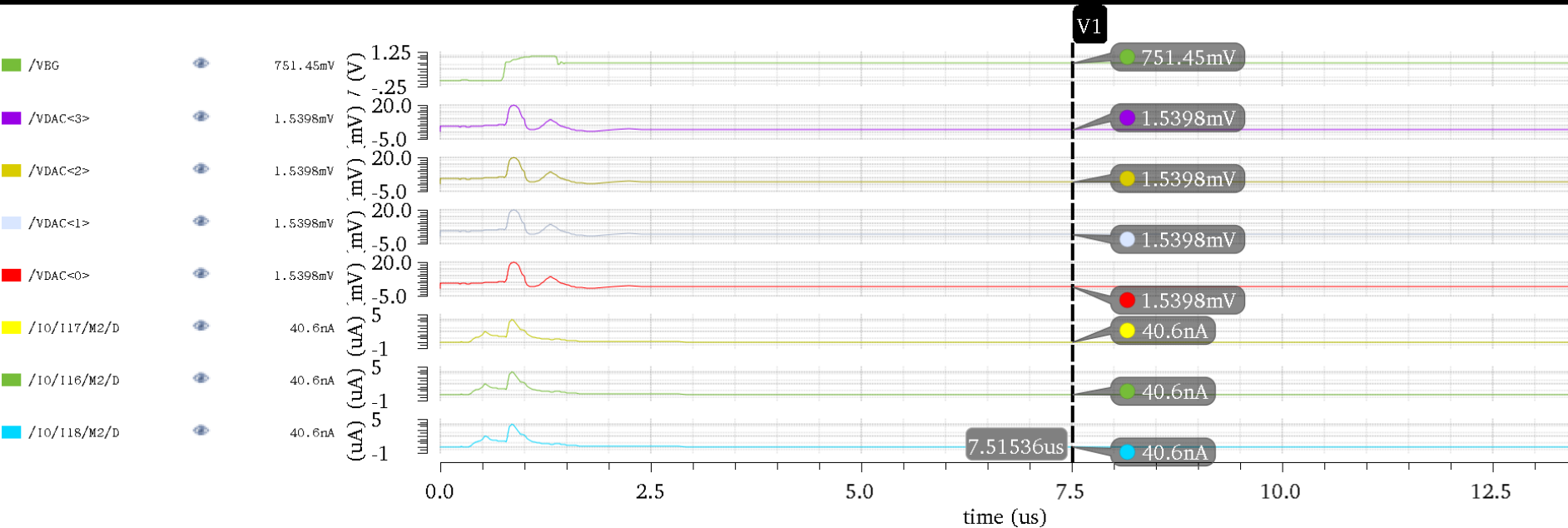


INL误差 消除增益误差



Simulation results of top circuit

Transient Response



■ Characteristics

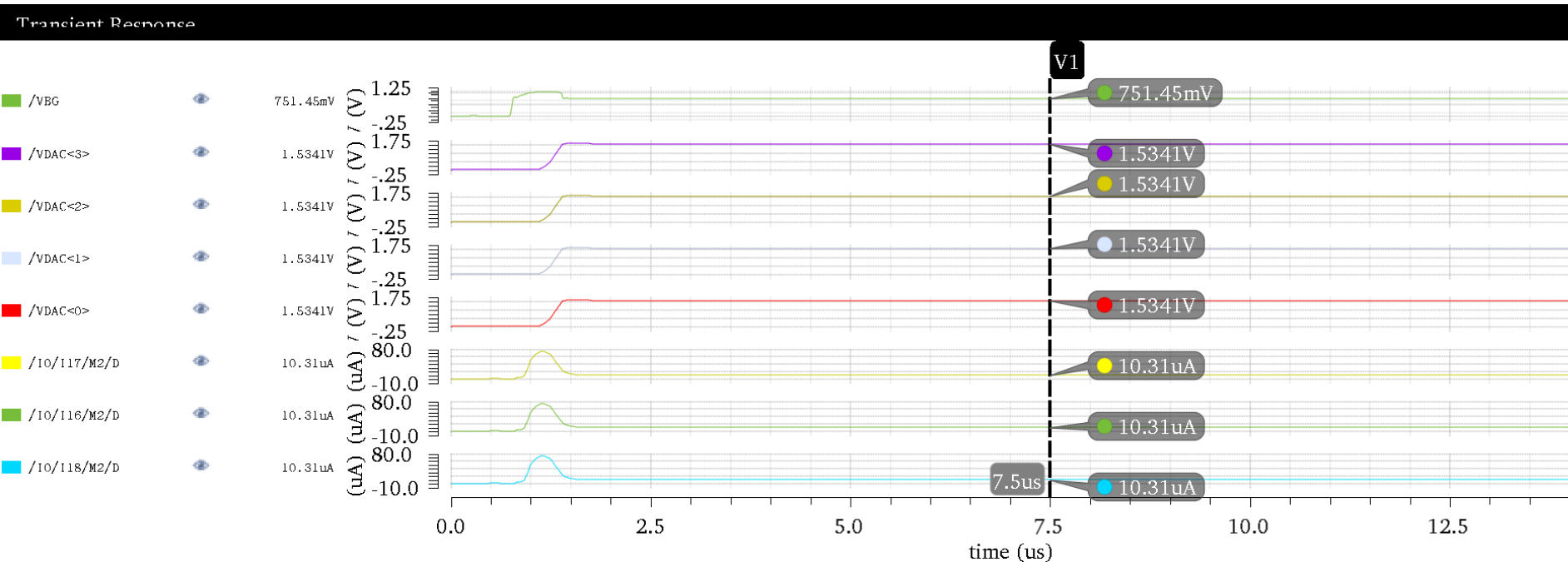
↳ Voltage DAC (VDAC)

- 10 bit
- LSB: 1.56 mV
- Range: 0 – 1.6 V

↳ Current DAC (CDAC)

- 8 bit
- LSB: 40 nA
- Range: 0 nA ~ 10.2 μ A

Simulation results of top circuit



■ Characteristics

↳ Voltage DAC (VDAC)

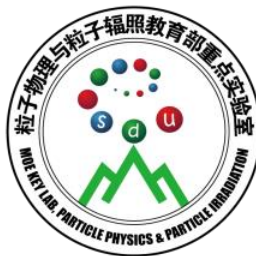
- 10 bit
- LSB: 1.56 mV
- Range: 0 – 1.6 V

↳ Current DAC (CDAC)

- 8 bit
- LSB: 40 nA
- Range: 0 nA ~ 10.2 μ A



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Thanks for your attention