Time and Frequency Distribution Method for LHAASO

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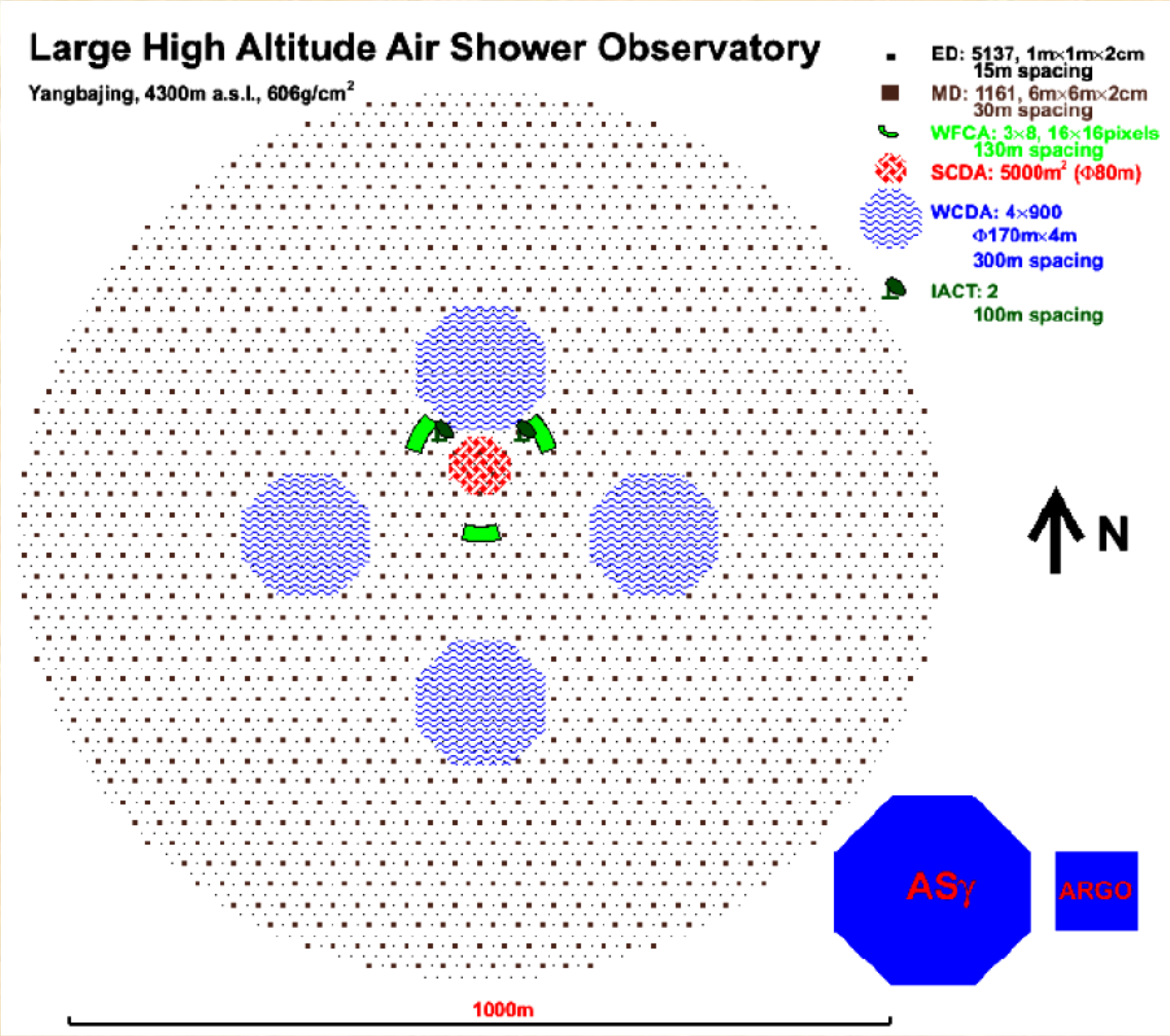
Outline

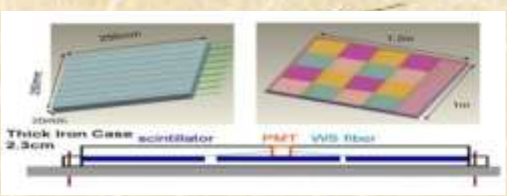
- LHAASO timing requirement
- Problems, challenges and solutions:
  - Existing technologies in IT industry and HEP;
  - Statement of possible solution;
- White Rabbit Protocol
  - Concept and Status
- Work to do
- Project Plan

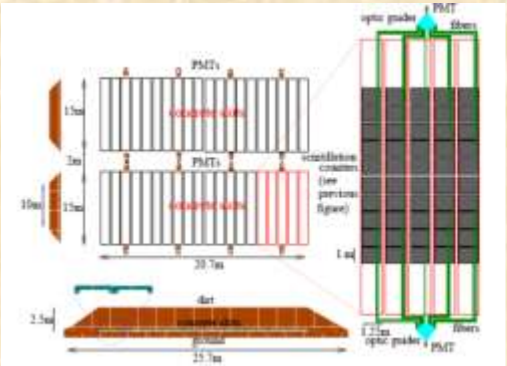
LHAASO Timing budget

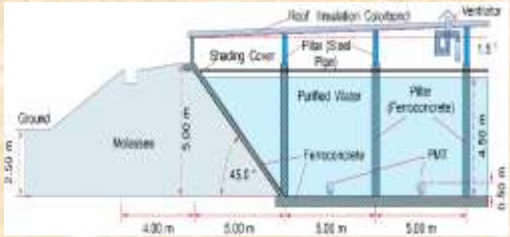
- 10k detectors and hundreds of DAQ nodes over 1 km^2;
- Sub-nanosecond timing accuracy;
- LHAASO Detectors:
  - KM2A:
    - Ground detector array over 1 km^2;
    - 5137 electron detectors, 15m gap;
    - 1200 μ detectors, 30m gap;
  - WCDA: (Water Cherenkov Detector Array)
    - 4 sites, 150m by 150m each;
    - 900 detectors in each site, 3600 in total;
  - WFCTA: Wide Field Cherenkov Telescope Array
    - 24 telescopes
  - SCDA: Shower Core Detector Array
    - Centered 5000 m^2 detector array

LHAASO Detector map









Timing system features needed

- Range and Scalability
  - Spreading 1km^2;
  - 10k detectors readout via hundreds of DAQs;
  - Precise time and frequency reference for each node;
  - Sub-nanosecond timing accuracy;
- Topology and Traceability
  - Master – slave, switches;
  - Share DAQ network medium;
- Robustness and Cost
  - Simple complexity and maintenance free;
  - Continuously working at high altitude in large temperature range with good power efficiency;
- Compatibility
  - Easy to integrate with DAQ system;
  - Compatible with industry standards;

Idea

- Functionality
  - Master / slave structure;
  - Frequency distribution and clock recovery;
  - Phase measurement and feedback control;
  - Real time continuous delay calibration;
  - Combined data/timing trasmit;

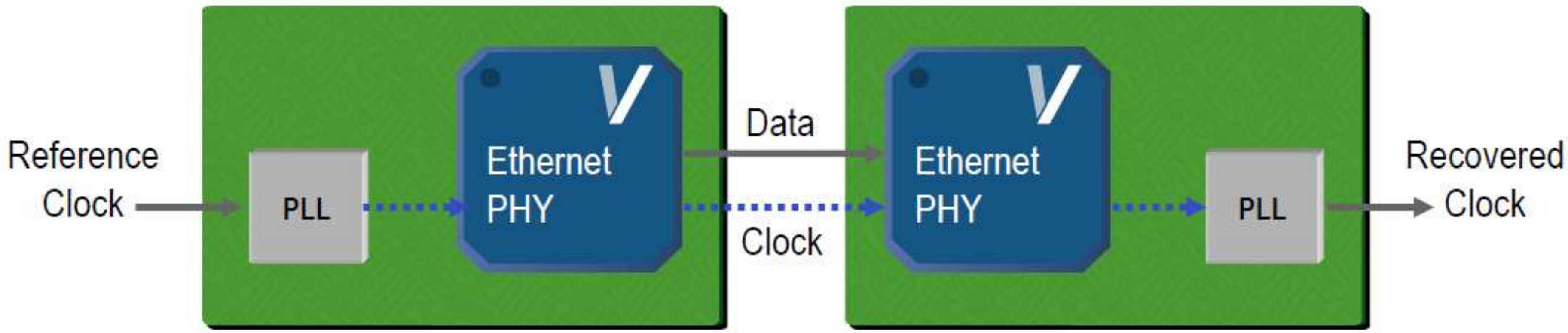
Evolution of time/freq distribution methods

Method	Ability	Accuracy jitter	Medium	Layer	Complexity	Manageability
Radio Clock	Time	10ms	Wireless	Layer 1	Simple	No
NTP	Time	1ms	Wireless	Layer 3	Complex	No
CDMA	Time/Freq	10µs	Wireless	Layer 2	Complex	?
WCDMA	Time/Freq	3µs	Wireless	Layer 2	Complex	?
WiMAX/ LTE	Time/Freq	1µs	Wireless	Layer 2	Complex	?
GPS	Time/Freq	14ns	Sat – earth	Layer 1	Simple	No
PTPv2	Time	~ns	Ethernet	Layer 2	Complex	Yes
UTI J.211	Time/Freq	1ns	Cable	Layer 1	Simple	Yes
SDH/SyncE	Freq	10ps	Ethernet	Layer 1	Simple	No
White Rabbit	Time/Freq	<1ns	Fiber GBE	Layer 1, 2	Complex	Yes
Optical carrier sync	Freq	<50fs	Fiber	Layer 1	Ultra complex	Yes
Optical Frequency Comb distribution	Time/Freq	<10fs	Fiber	Layer 1	Ultra complex	Yes

Synchronous Ethernet (SyncE)

- Extends SONET/SDH Layer 1 timing concepts to Ethernet networks
  - Clock distribution method similar to SONET/SDH
  - Clock timing requirement adapted from SONET/SDH specification
  - Supports Clock Failover/Holdover through Synchronization Status Message (SSM) byte messaging
    - Failover: If primary node fails, then secondary node is backup
    - Holdover: Switch over to Local Reference Clock if primary and secondary nodes fail
- Guarantees precise frequency resolution
- All nodes must have a clock source traceable to a Primary Reference Clock (PRC)
  - Clock source can be derived from incoming data OR an independent clock source
  - An external PLL can be used for frequency correction on each local node

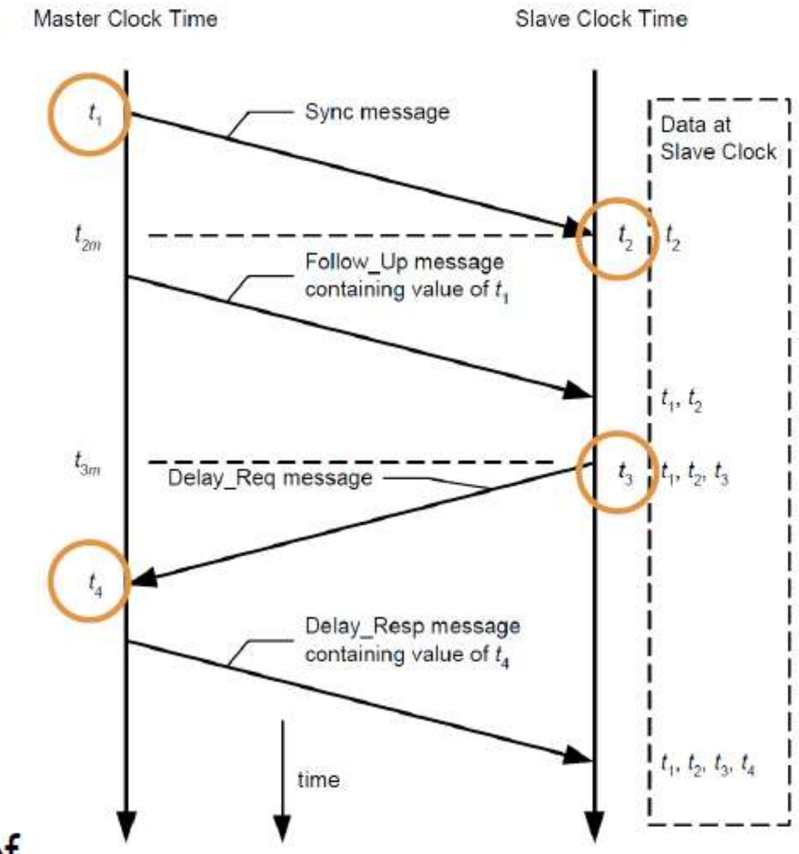
Synchronous Ethernet Timing Overview



- Synchronization is based on a primary reference clock (PRC) injected at the transmitter end
- Clock timing is distributed by way of downstream node clock recovery from the transmitted data
- Use of the PLL for clock recovery helps reduce jitter propagation in noisy network environments

IEEE1588 Timing Overview

- In IEEE1588, Time of Day (ToD) is distributed in frames as indicated in the figure
- By sending out time-stamped frames, delay and offset can be calculated as follows:
  - t2 - t1 = Delay + Offset
  - t4 - t3 = Delay – Offset
  - Delay = (t2 – t1 + t4 – t3) / 2
  - Offset = (t2 – t1 – t4 + t3) / 2
- IEEE1588 can be used together with SyncE to ensure high quality transport of timing information across the network



The White Rabbit Project

- A Protocol proposed by CERN, GSI
- Features:
  - Open source, SW & HW;
  - Sync-E + PTPv2 + WR;
  - Determinism, high priority packet delay kept in certain time period;
  - Clock recovery and phase tracking;
  - Sub-ns accuracy;
  - Up to 1000 nodes;
- Status:
  - Kicked off in 2008;
  - Demo 1st switch 2010/10;
  - 2011.1: 10km fiber test, pll verification;
  - 2011 Q3: WR switch V3;
  - 2012 Q3: Release commercial product;

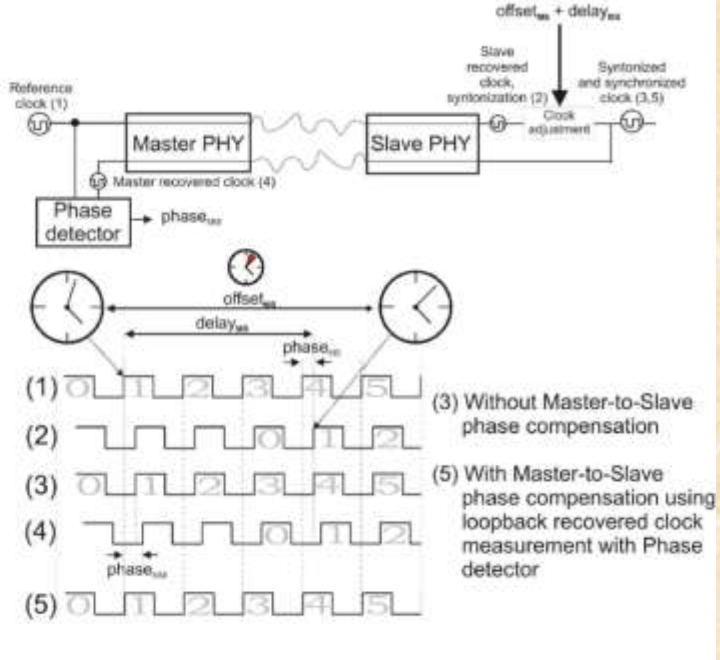
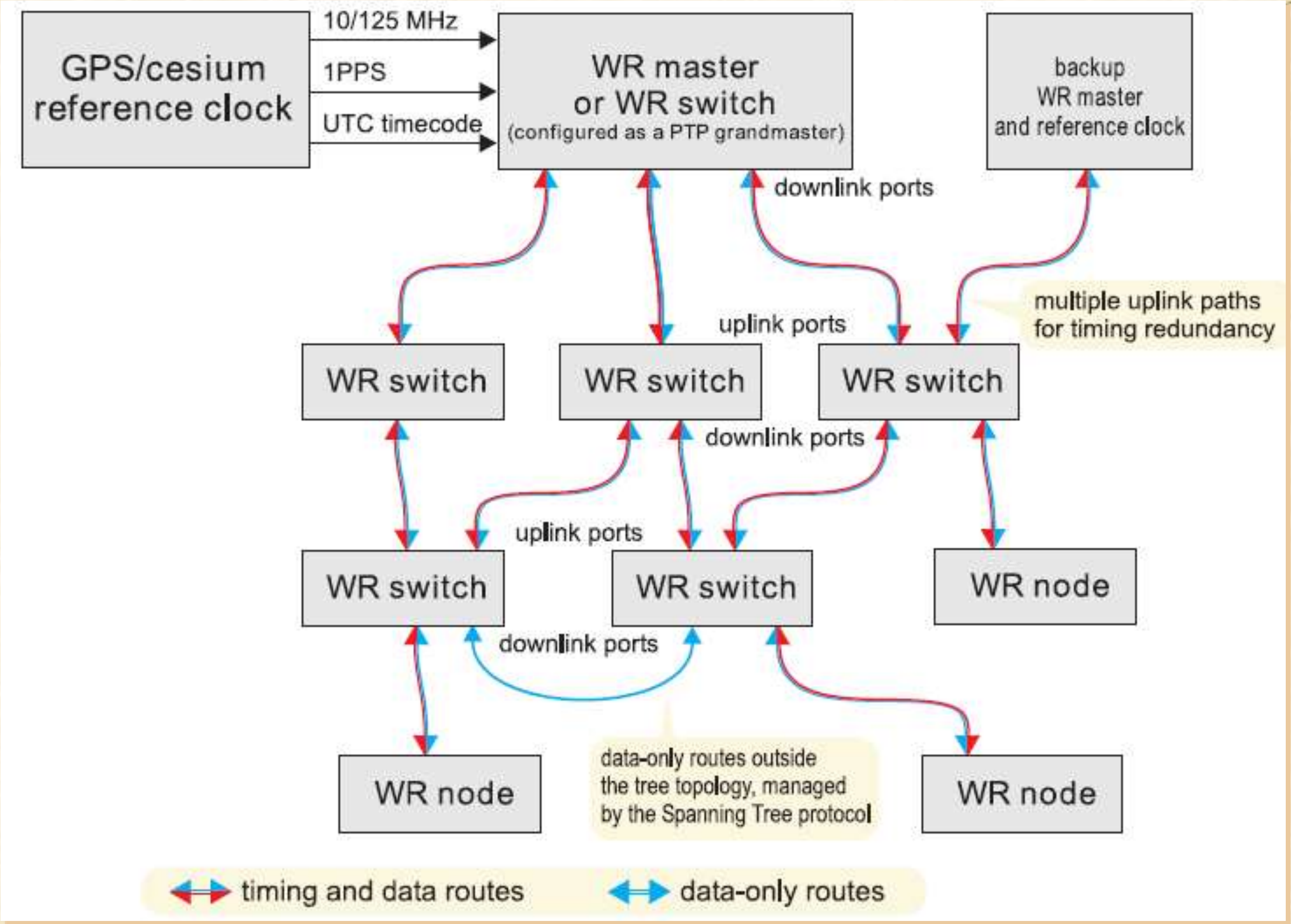
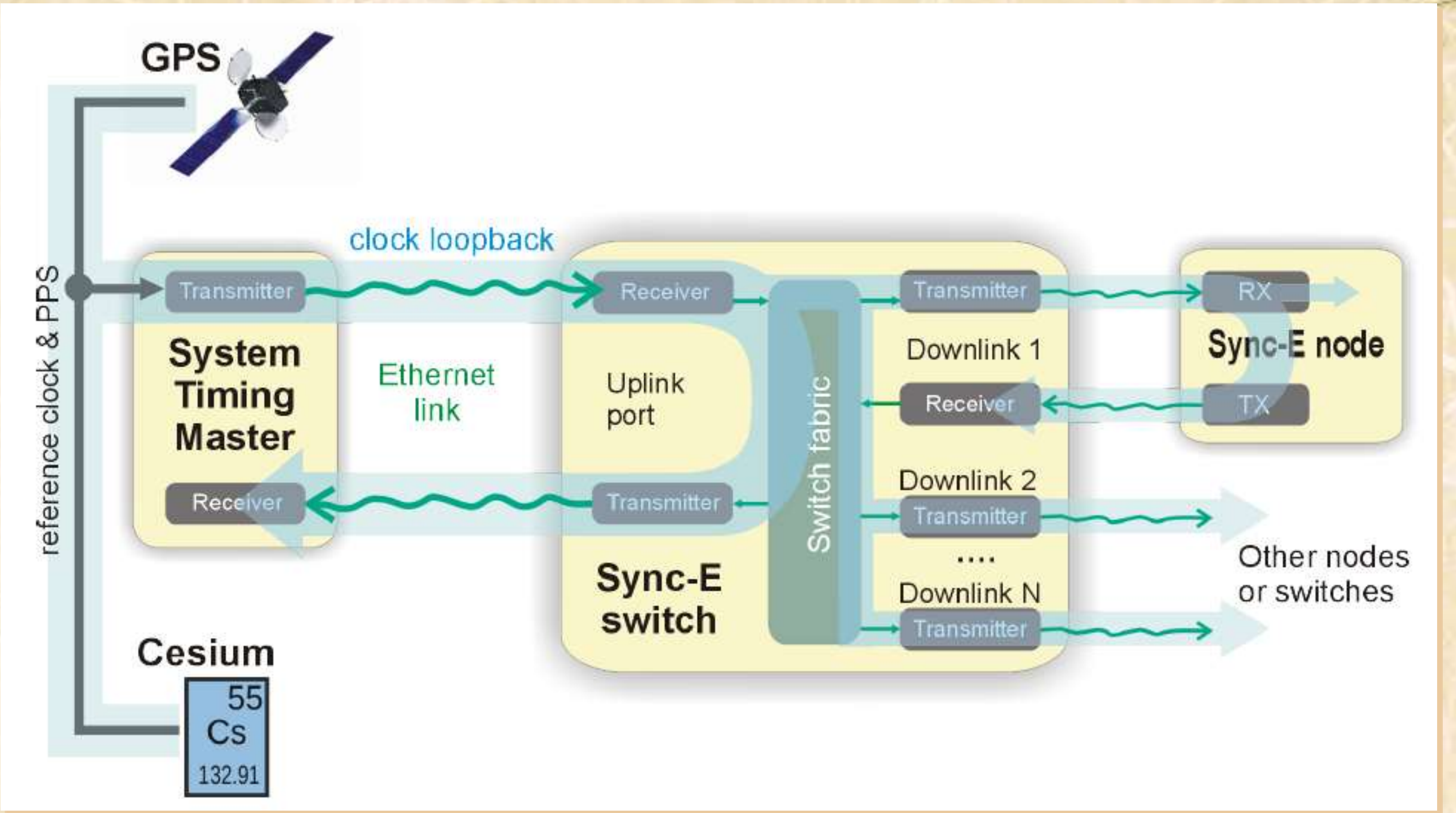


Figure 1: Synchronization and syntonization in a White Rabbit link.

White Rabbit Network Topology



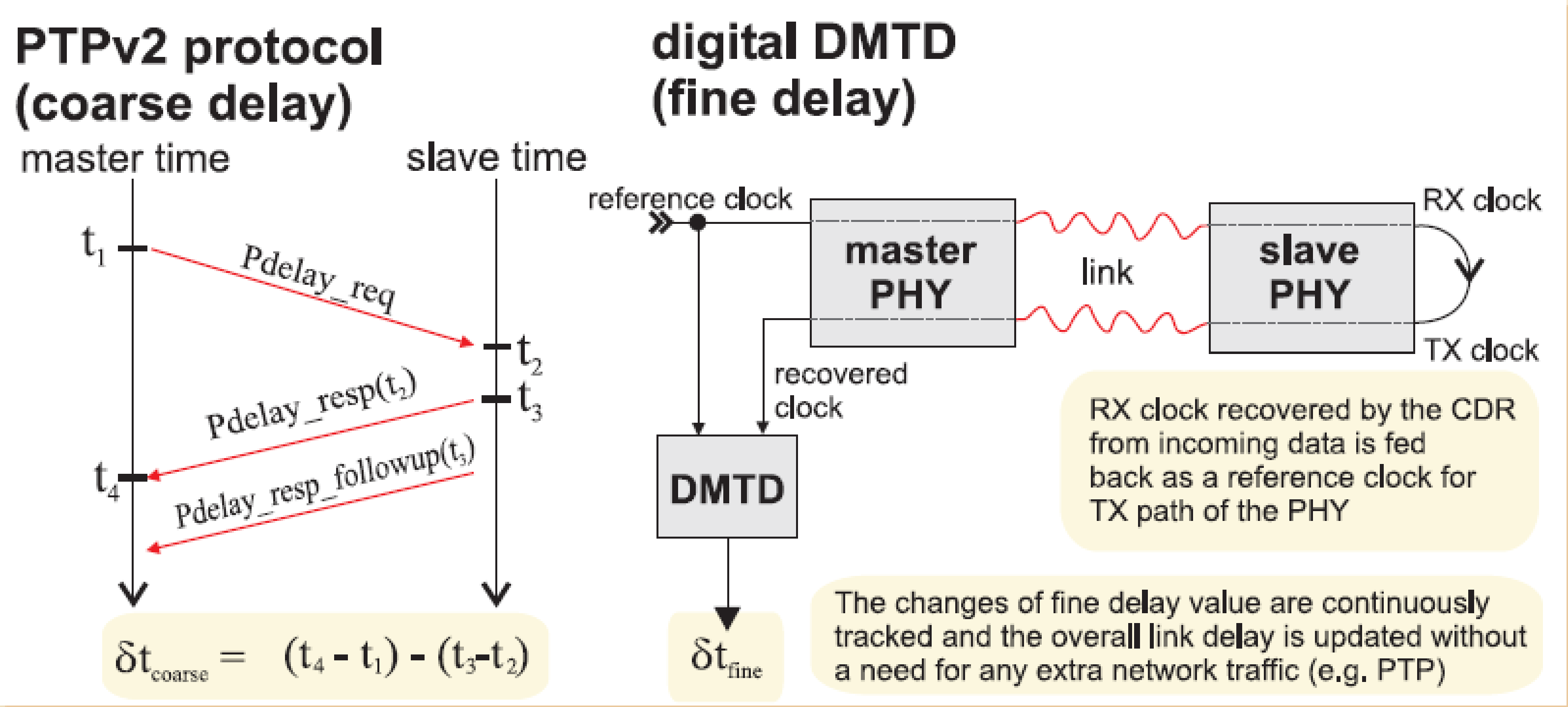
Sync-E and Phase Tracking



- PTP alone is not good enough;
- Measure phase shift between TX and RX on master side;

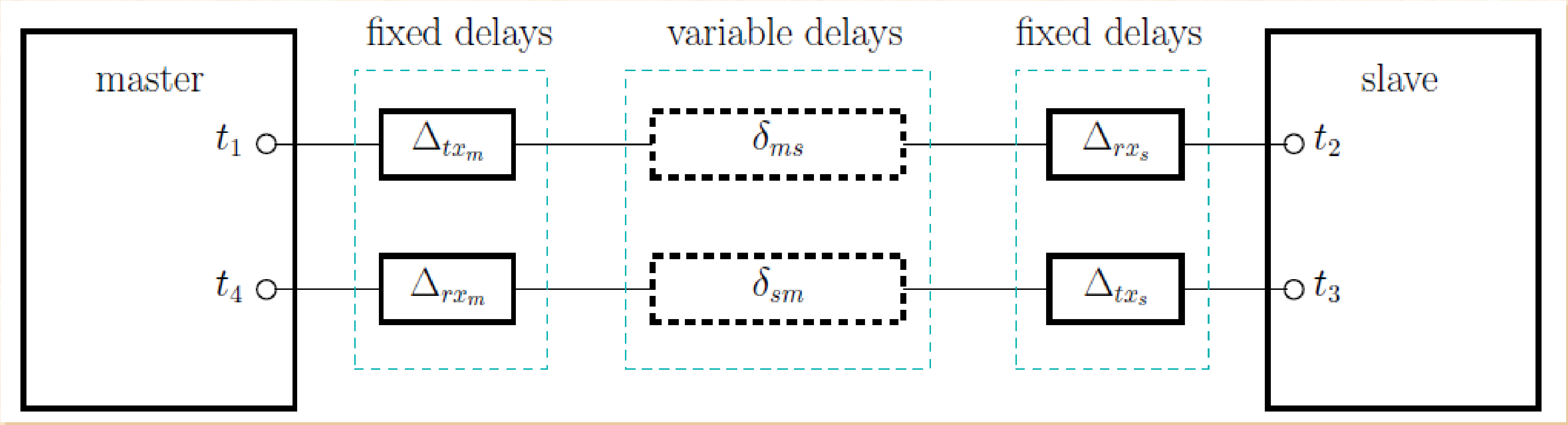
Enhanced PTP (IEEE 1588-2008)

- Synchronizes local clock with master by calibrating the delay introduced by link.



Link Delay Model

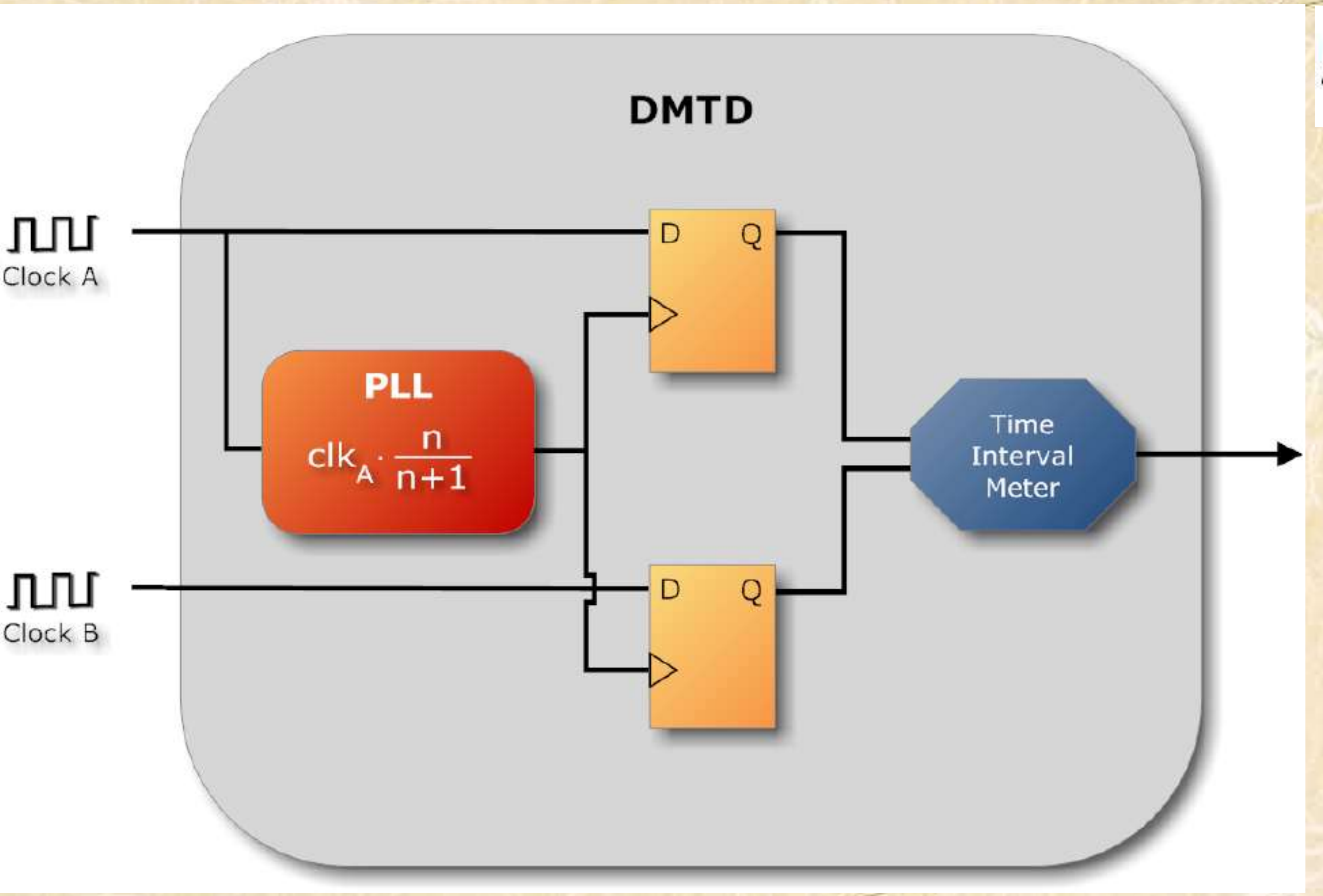
- Delay asymmetry calculation;
- WR PTP extension for fixed delay calibration;



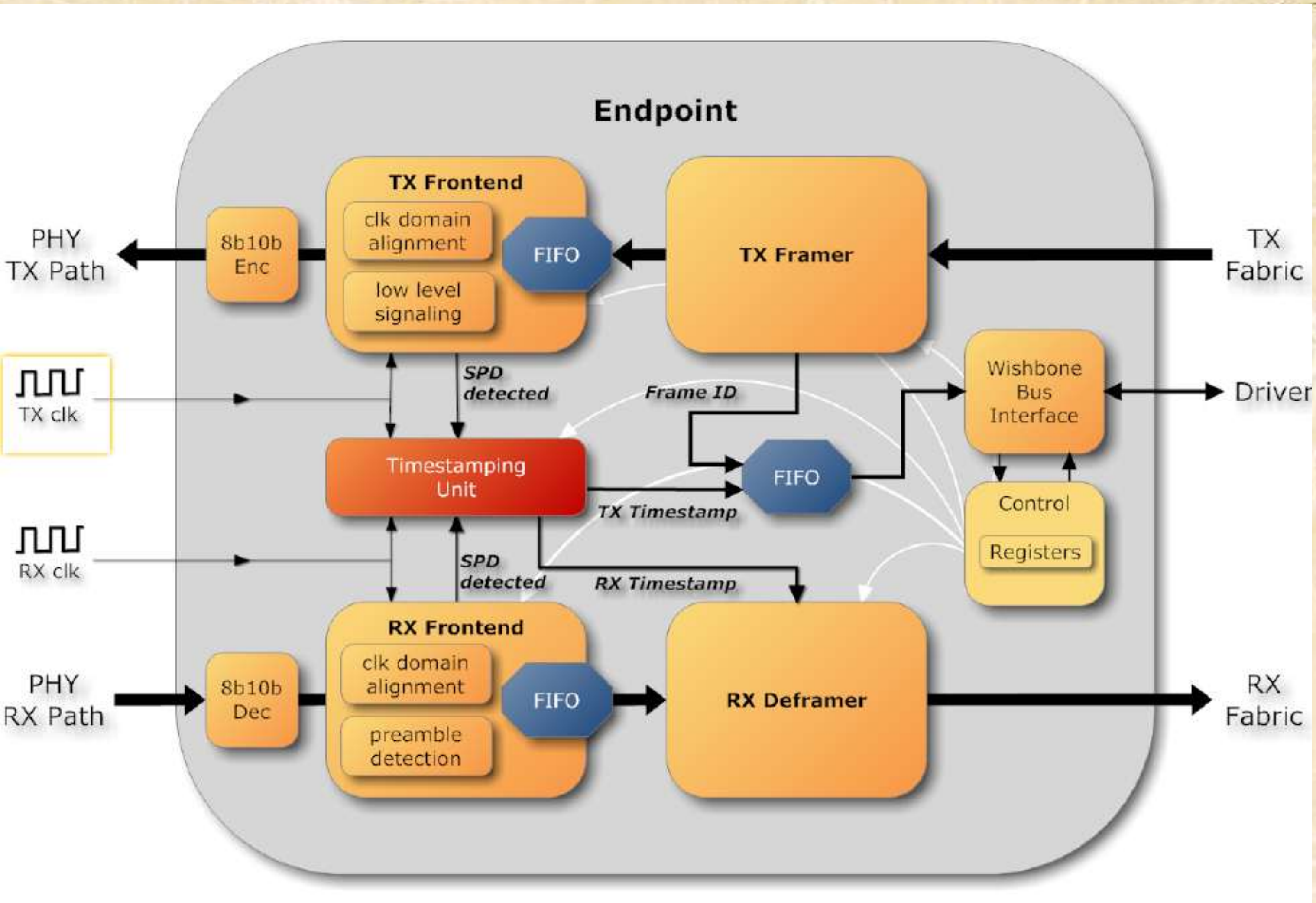
Work to do

- Topology design
  - Master reference system;
  - Sharing data link topology;
- WR implementation
  - Hardware
    - WR switch co-development;
    - WR nodes co-development;
    - Measurement instrumentation;
  - HDL
    - Sync-E clock recovery and DDS;
    - DMTD phase measurement;
  - Software
    - Linux OS;
    - PTP Daemon;
    - Management console;
  - Simulation
- System Integration
  - Time-stamping;
  - Clock management;
  - Central management;
- Testing
  - Performance testing;
  - Reliability testing;
  - Robustness testing;
  - DAQ testing;
- Documentation
- Fabrication
- Deployment
- Verification

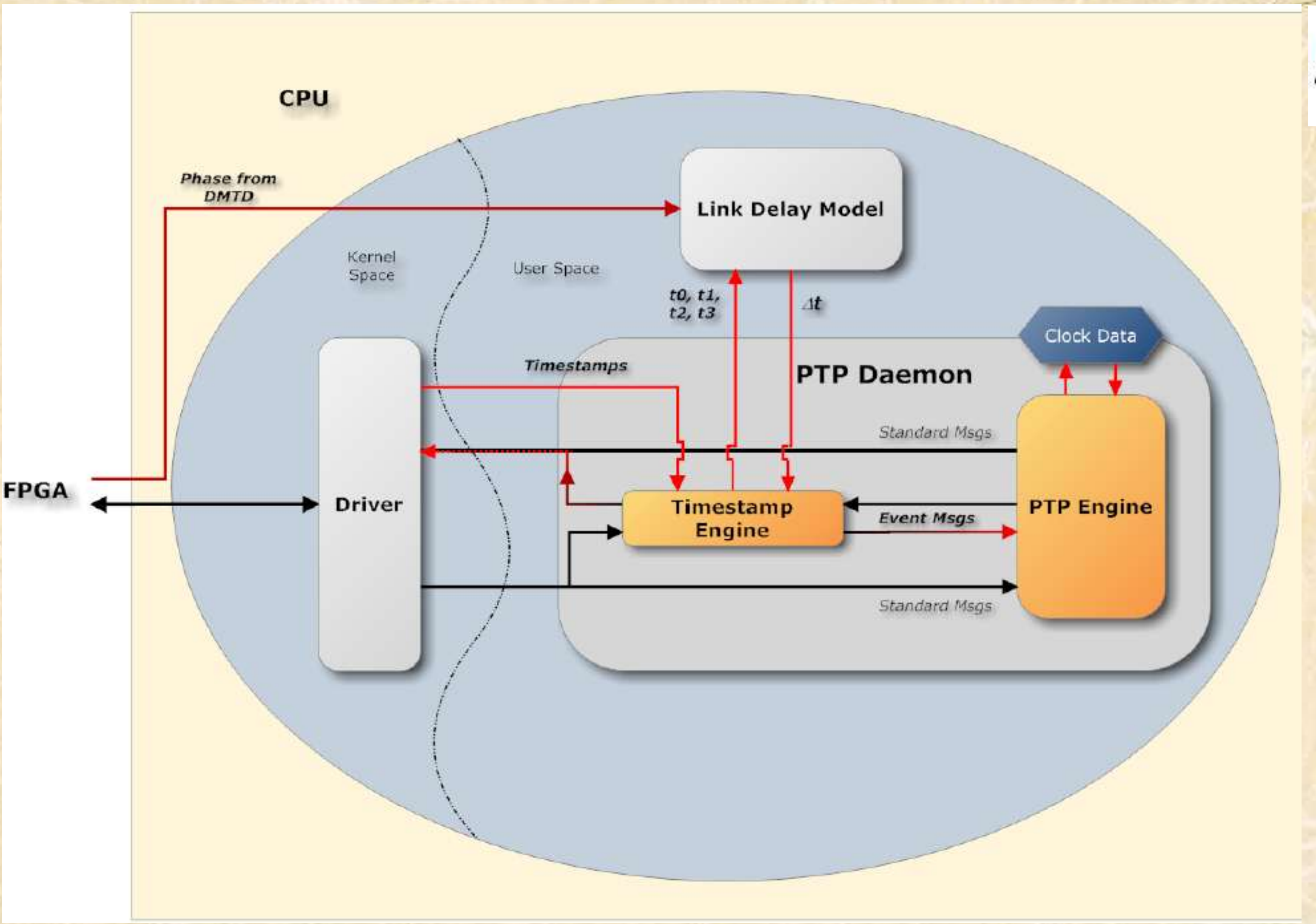
Phase tracking HDL



Sync-E HDL


Endpoint
TX Frontend
clk domain alignment
low level signaling
FIFO
TX Framer
PHY TX Path
8b10b Enc
TX Fabric
TX clk
SPD detected
Frame ID
Wishbone Bus Interface
Driver
Timestamping Unit
FIFO
TX Timestamp
Control
Registers
RX clk
SPD detected
RX Timestamp
RX Frontend
clk domain alignment
preamble detection
FIFO
RX Deframer
PHY RX Path
8b10b Dec
RX Fabric

Software PTP Daemon



Status and Plan

• 2010.12:	First contact;
• 2011.1.27:	First discussion & organization;
• 2011.2:	Project Start;
• 2011.6:	Topology & implementation design;
• 2011.12:	Key tech Verification & simulation;
• 2012.Q2:	WR implementation;
• 2012 Q4:	Hardware fabrication & test;
• 2013:	Integration and deployment;
• 2014:	System test;

Questions?

谢谢！